FIG. 1

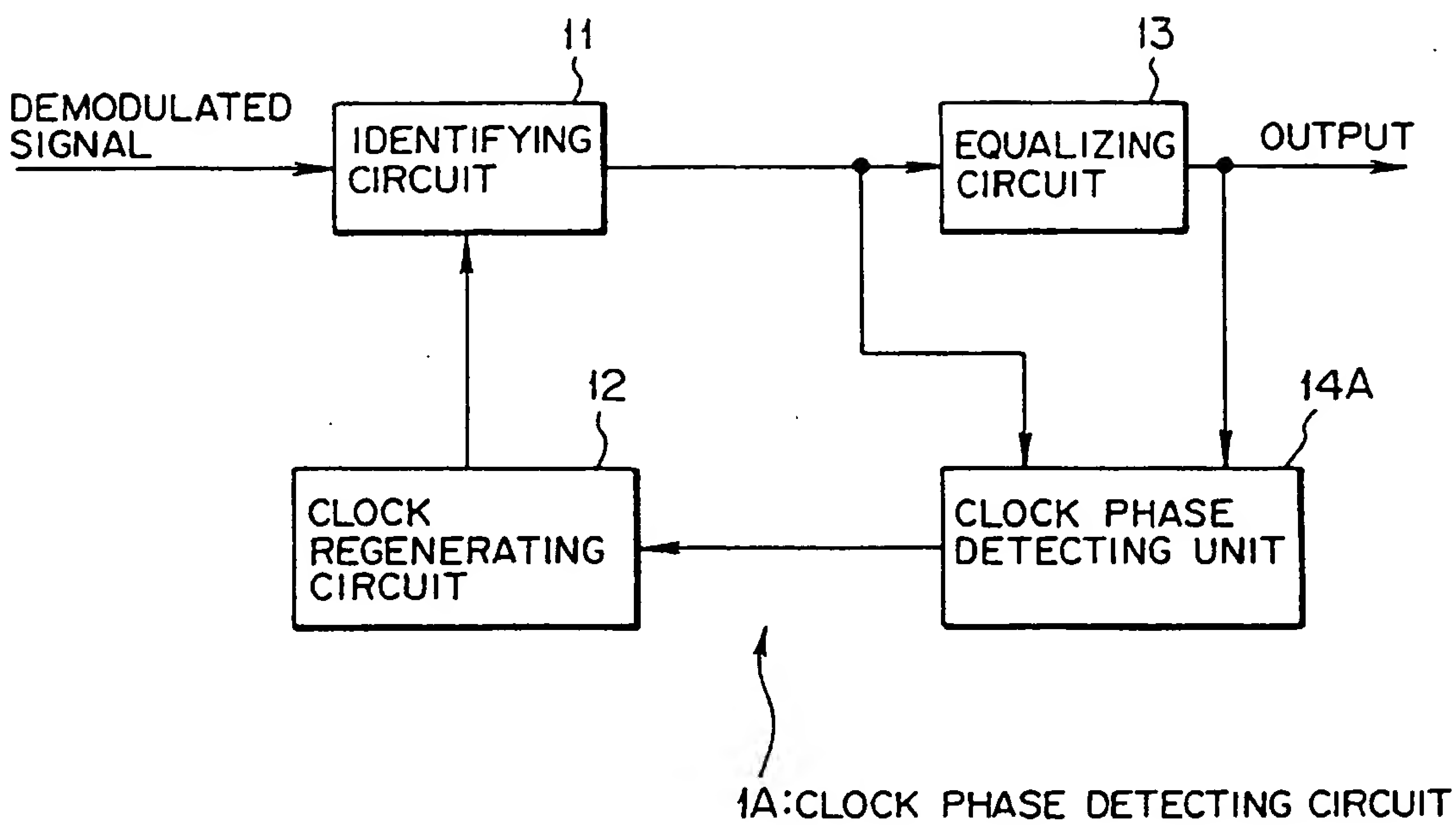


FIG. 2

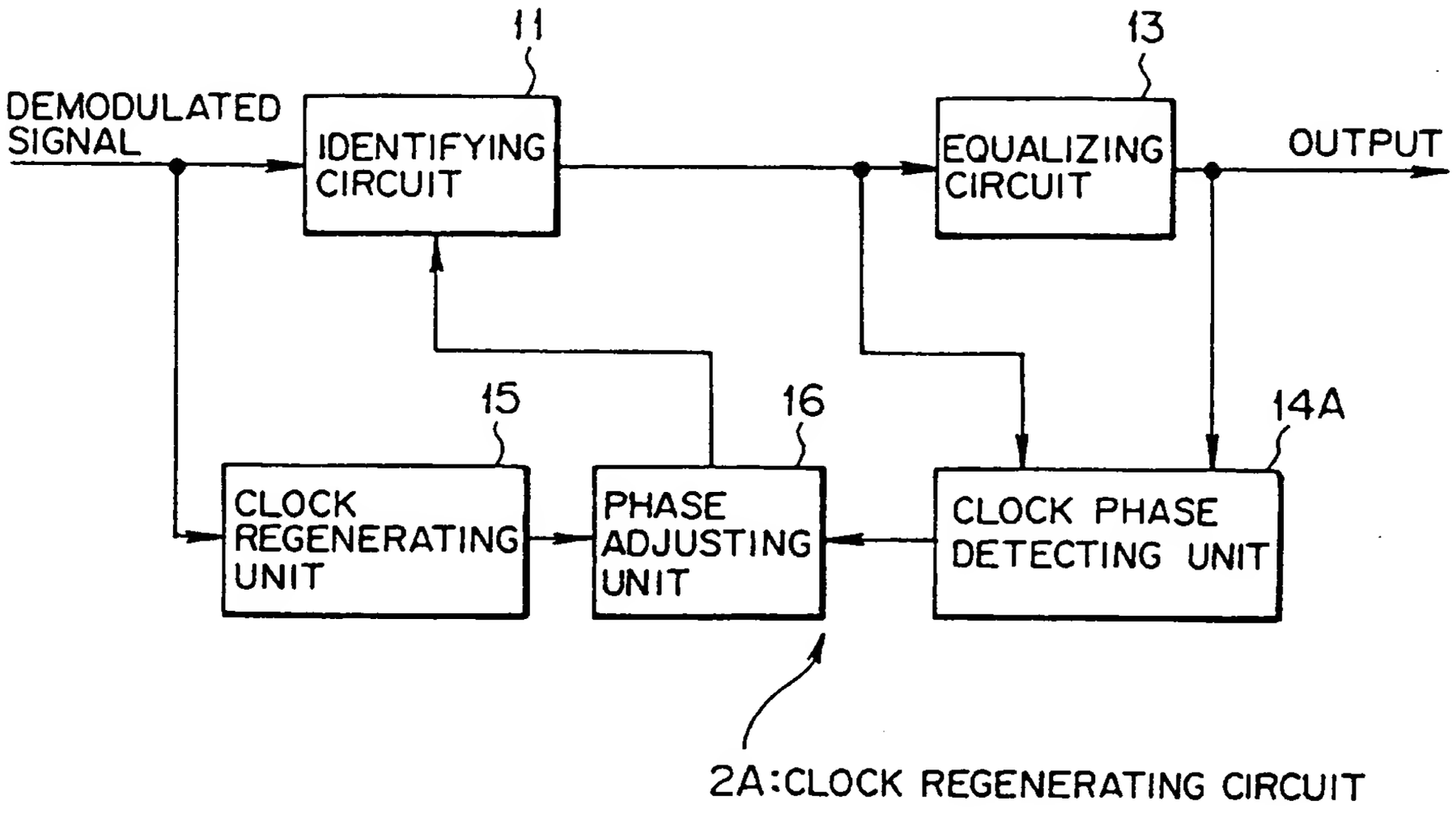

11
13
DEMODULATED SIGNAL
IDENTIFYING CIRCUIT
EQUALIZING CIRCUIT
OUTPUT
15
16
14A
CLOCK REGENERATING UNIT
PHASE ADJUSTING UNIT
CLOCK PHASE DETECTING UNIT
2A:CLOCK REGENERATING CIRCUIT

FIG.3

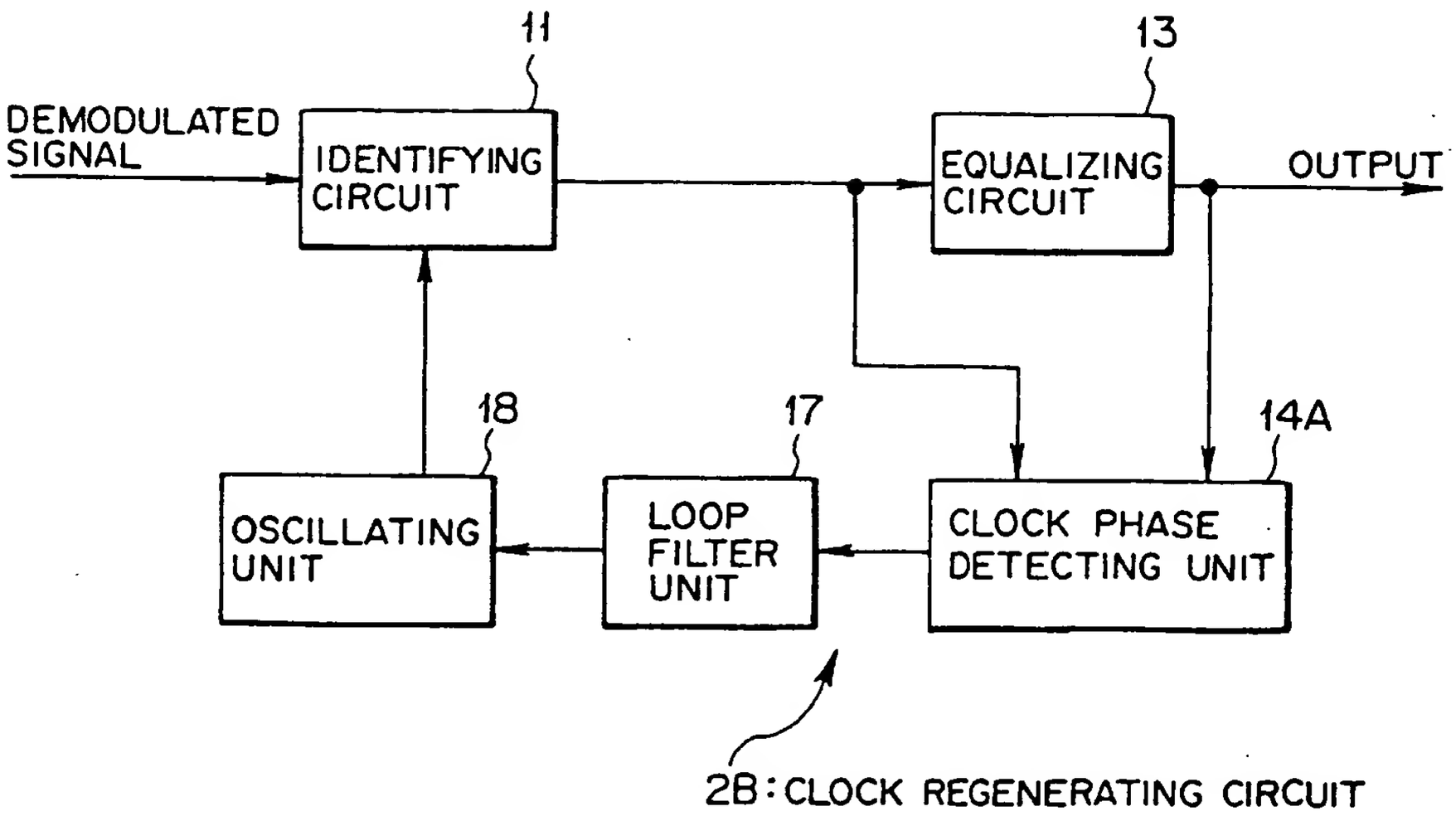

11
13
DEMODULATED SIGNAL
IDENTIFYING CIRCUIT
EQUALIZING CIRCUIT
OUTPUT
18
17
14A
OSCILLATING UNIT
LOOP FILTER UNIT
CLOCK PHASE DETECTING UNIT
2B: CLOCK REGENERATING CIRCUIT

FIG.4

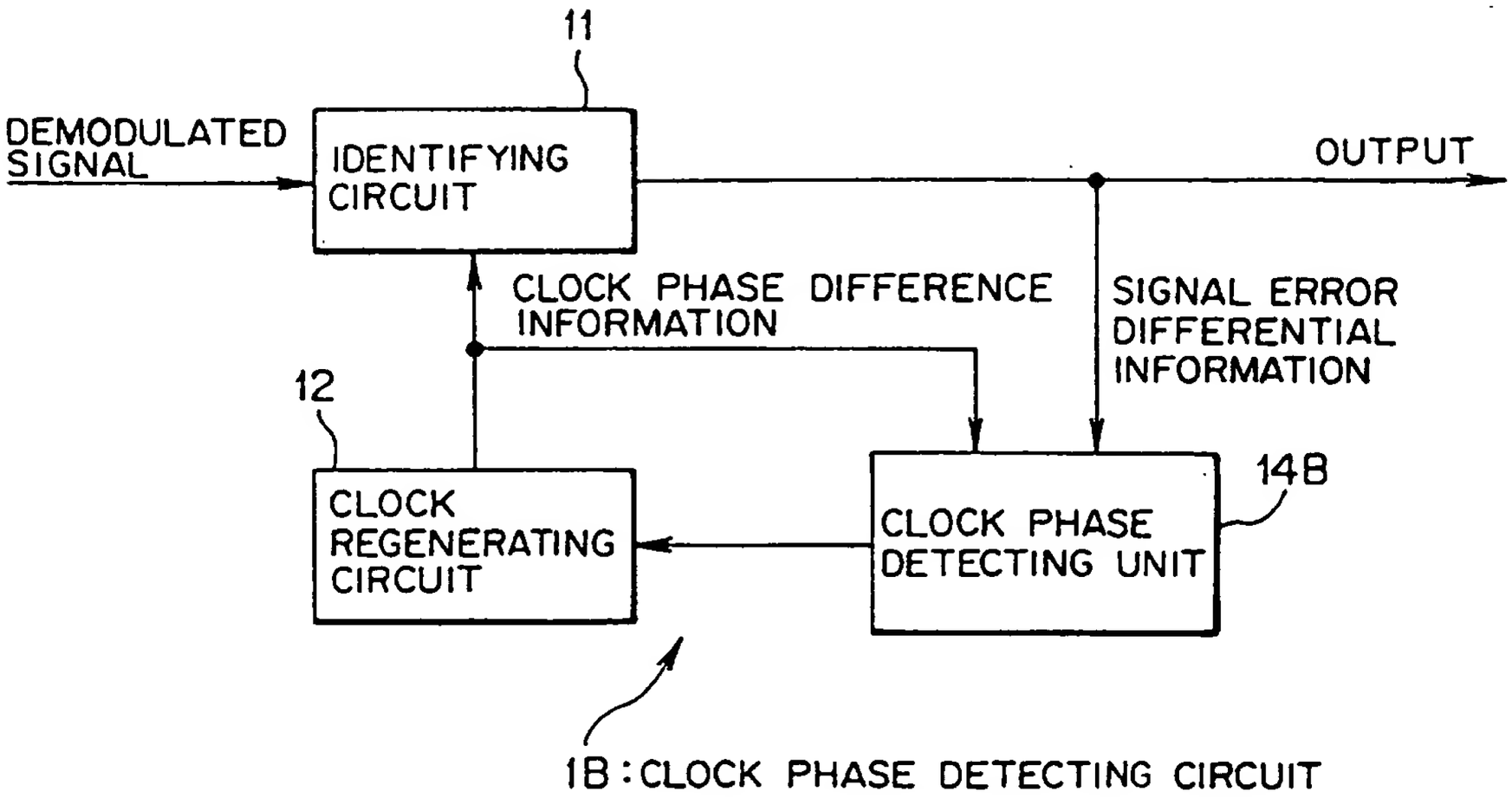

11
DEMODULATED SIGNAL
IDENTIFYING CIRCUIT
OUTPUT
CLOCK PHASE DIFFERENCE INFORMATION
SIGNAL ERROR DIFFERENTIAL INFORMATION
12
CLOCK REGENERATING CIRCUIT
14B
CLOCK PHASE DETECTING UNIT
1B : CLOCK PHASE DETECTING CIRCUIT

FIG.5

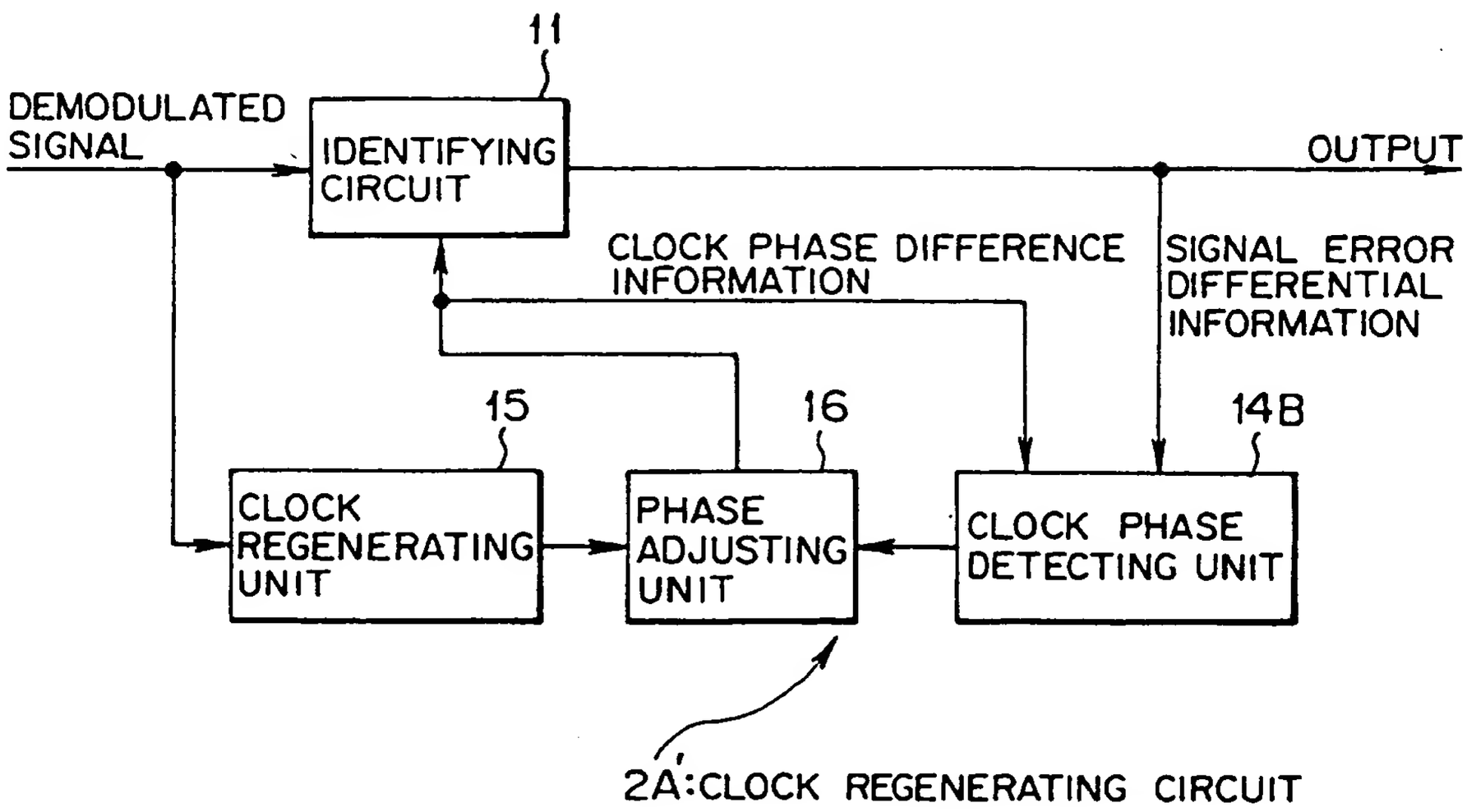

11
DEMODULATED SIGNAL
IDENTIFYING CIRCUIT
OUTPUT
CLOCK PHASE DIFFERENCE INFORMATION
SIGNAL ERROR DIFFERENTIAL INFORMATION
15
16
14B
CLOCK REGENERATING UNIT
PHASE ADJUSTING UNIT
CLOCK PHASE DETECTING UNIT
2A': CLOCK REGENERATING CIRCUIT

FIG.6

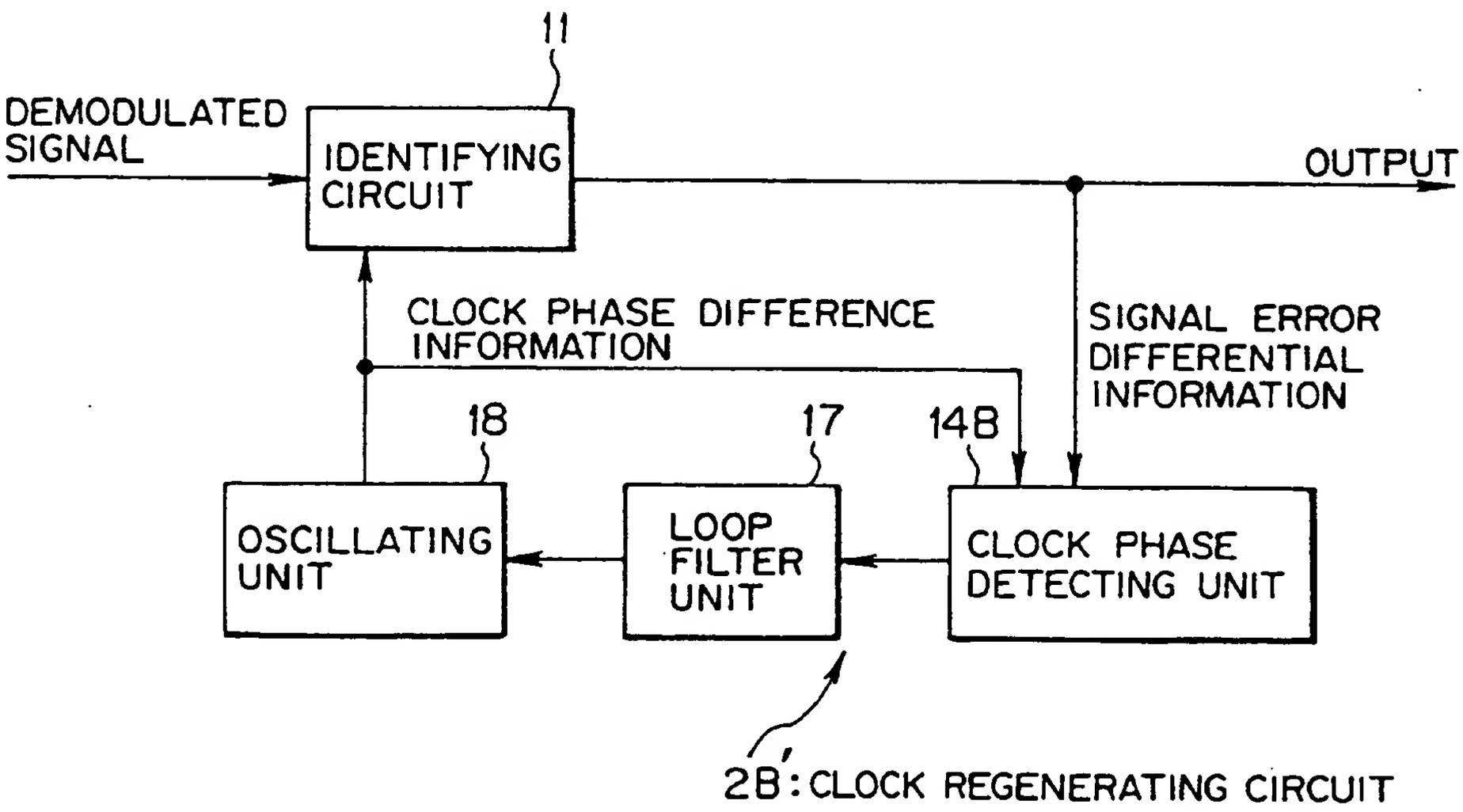

11
DEMODULATED SIGNAL
IDENTIFYING CIRCUIT
OUTPUT
CLOCK PHASE DIFFERENCE INFORMATION
SIGNAL ERROR DIFFERENTIAL INFORMATION
18
17
14B
OSCILLATING UNIT
LOOP FILTER UNIT
CLOCK PHASE DETECTING UNIT
2B': CLOCK REGENERATING CIRCUIT

FIG. 7

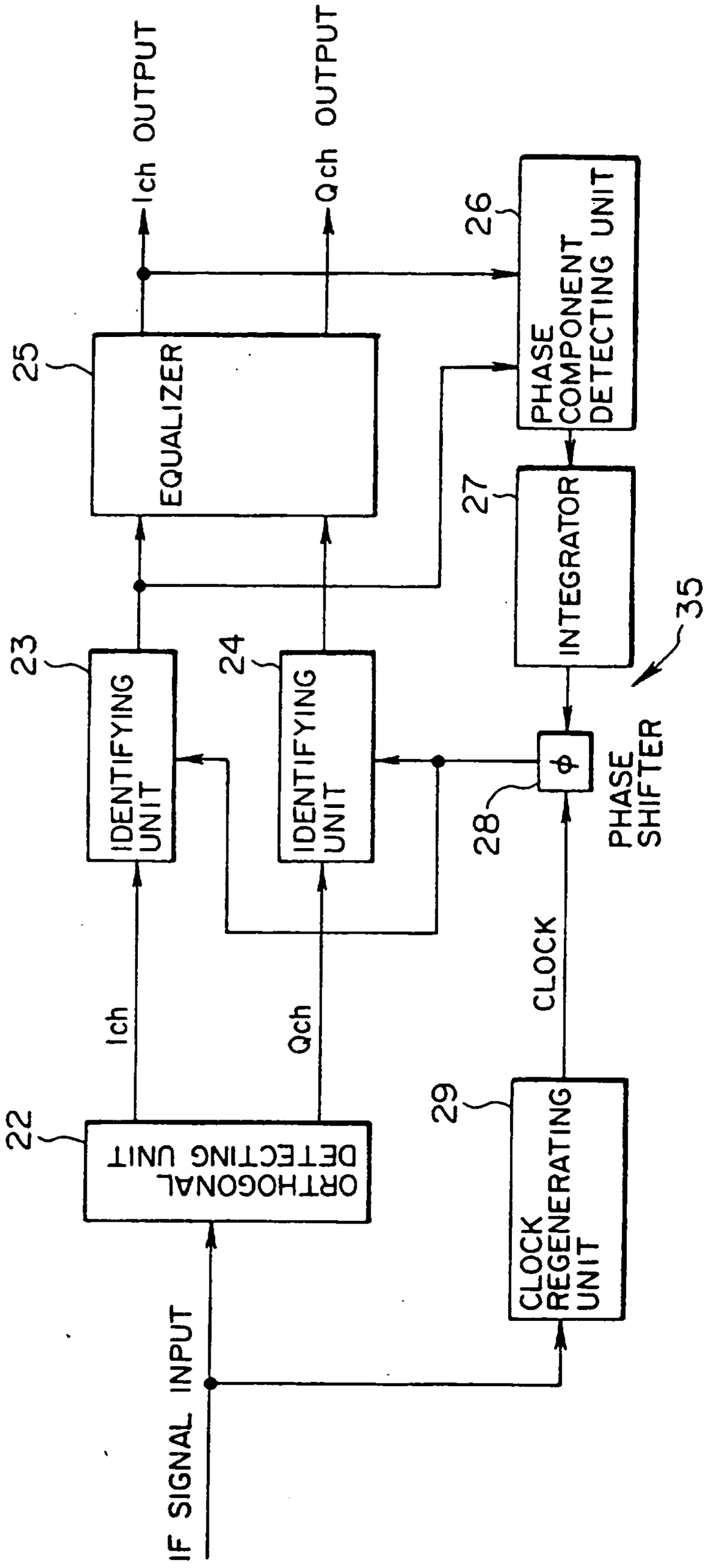

Ich OUTPUT
Qch OUTPUT
26
PHASE COMPONENT DETECTING UNIT
25
EQUALIZER
27
INTEGRATOR
35
23
IDENTIFYING UNIT
24
IDENTIFYING UNIT
28
φ
PHASE SHIFTER
Ich
Qch
CLOCK
22
ORTHOGONAL DETECTING UNIT
29
CLOCK REGENERATING UNIT
IF SIGNAL INPUT

FIG.8

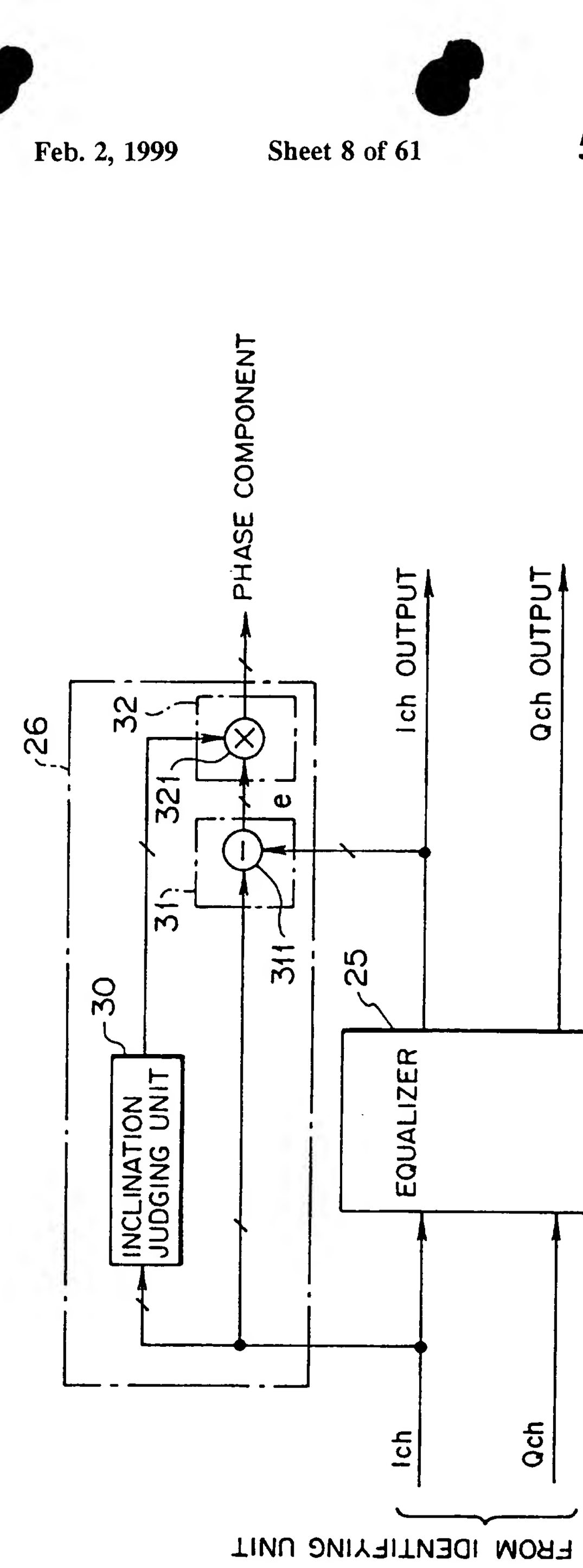

FROM IDENTIFYING UNIT
Ich
Qch
EQUALIZER
25
Ich OUTPUT
Qch OUTPUT
PHASE COMPONENT
26
32
321
311
e
30
INCLINATION JUDGING UNIT

FIG. 9

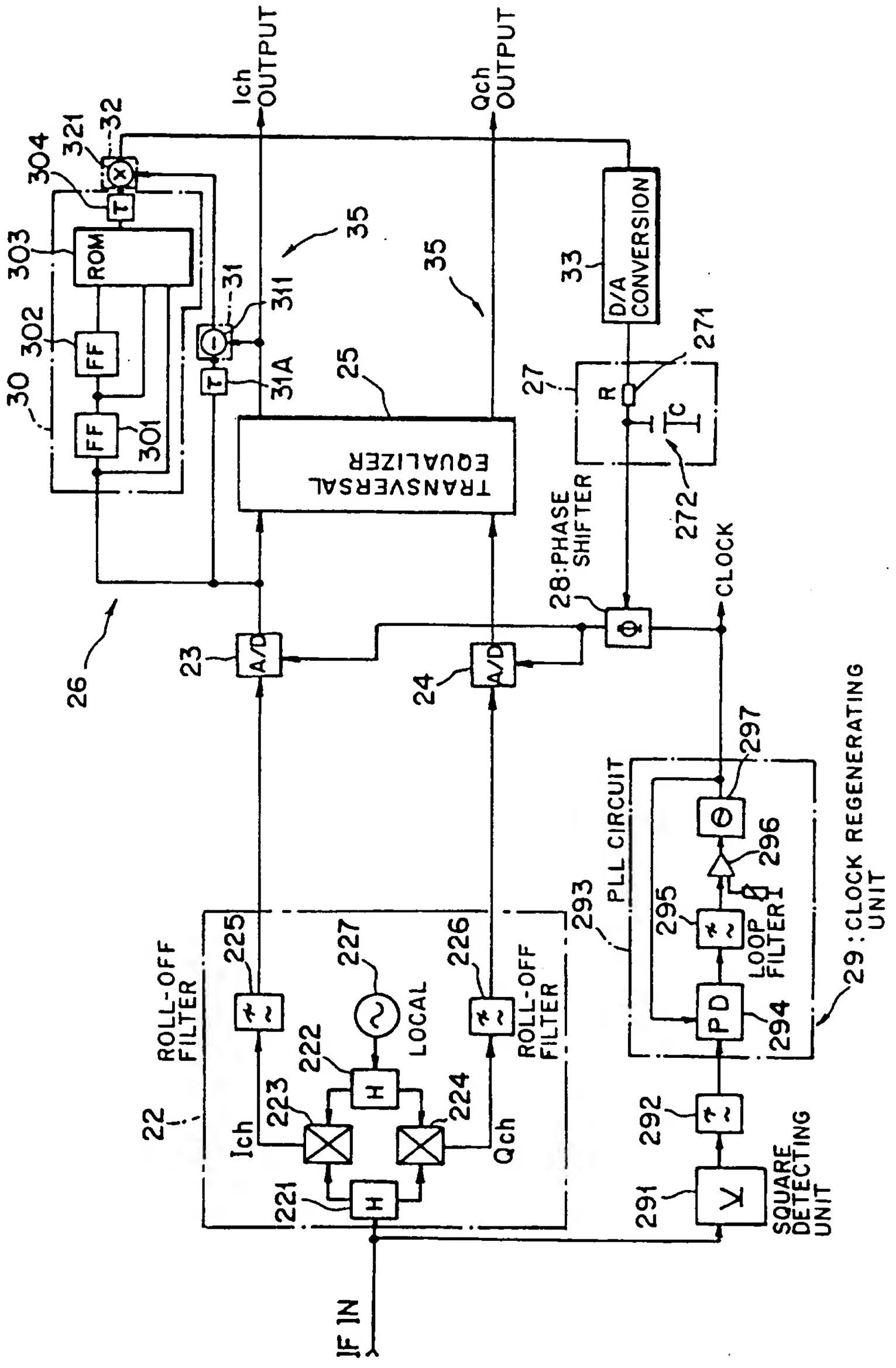

Ich OUTPUT
Qch OUTPUT
32
321
304
303
ROM
302
FF
FF
301
30
31
311
31A
35
25
TRANSVERSAL EQUALIZER
26
23
24
A/D
A/D
33
D/A CONVERSION
271
27
R
Tc
272
28:PHASE SHIFTER
Φ
CLOCK
297
Θ
296
PLL CIRCUIT
293
295
LOOP FILTER
PD
294
29:CLOCK REGENERATING UNIT
292
291
SQUARE DETECTING UNIT
22
ROLL-OFF FILTER
225
227
226
ROLL-OFF FILTER
LOCAL
222
223
224
221
Ich
Qch
IF IN

FIG. 10

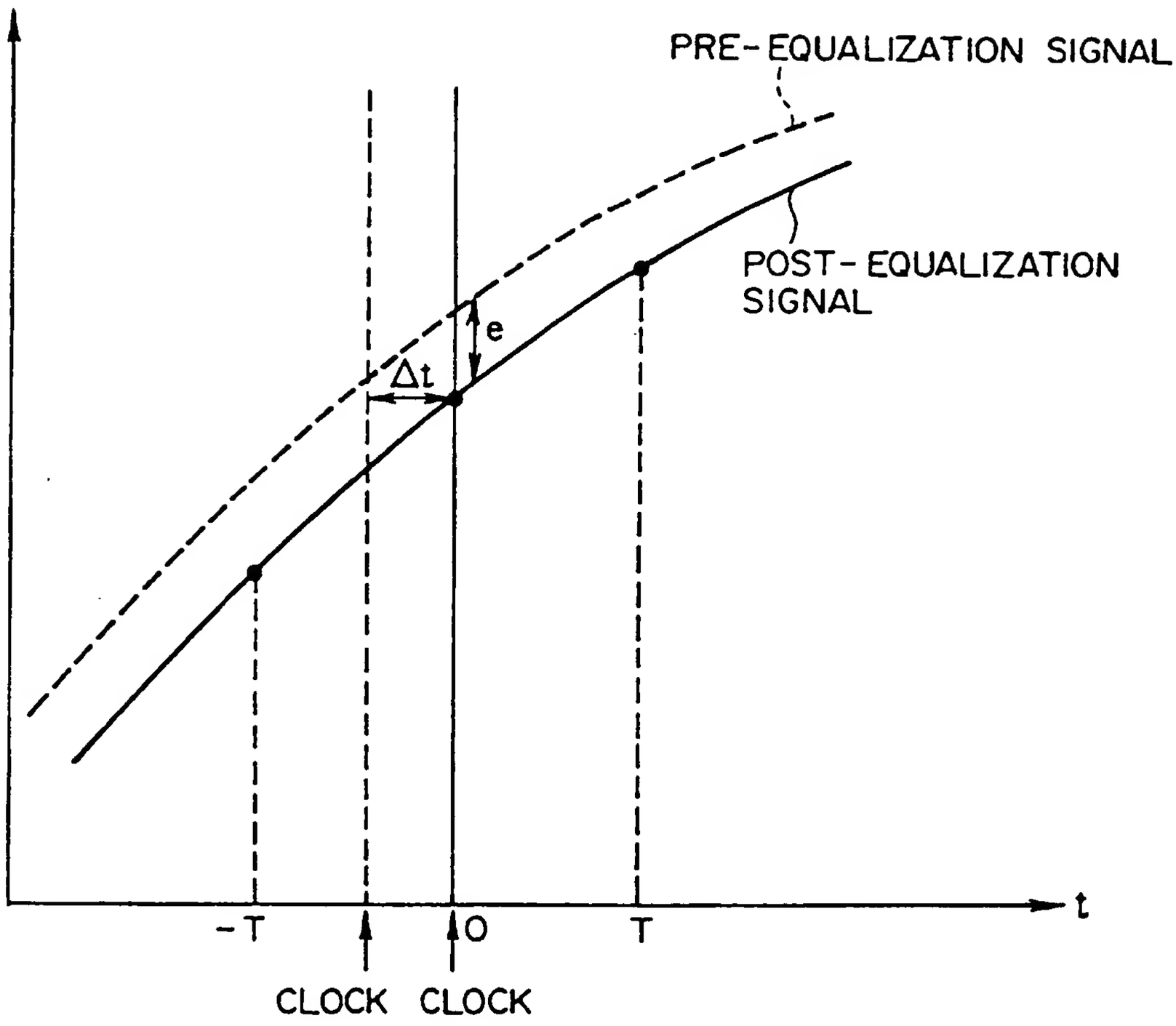

PRE-EQUALIZATION SIGNAL
POST-EQUALIZATION SIGNAL
SIGNAL LEVEL
e
Δt
t
-T
O
T
CLOCK
CLOCK

FIG. 11

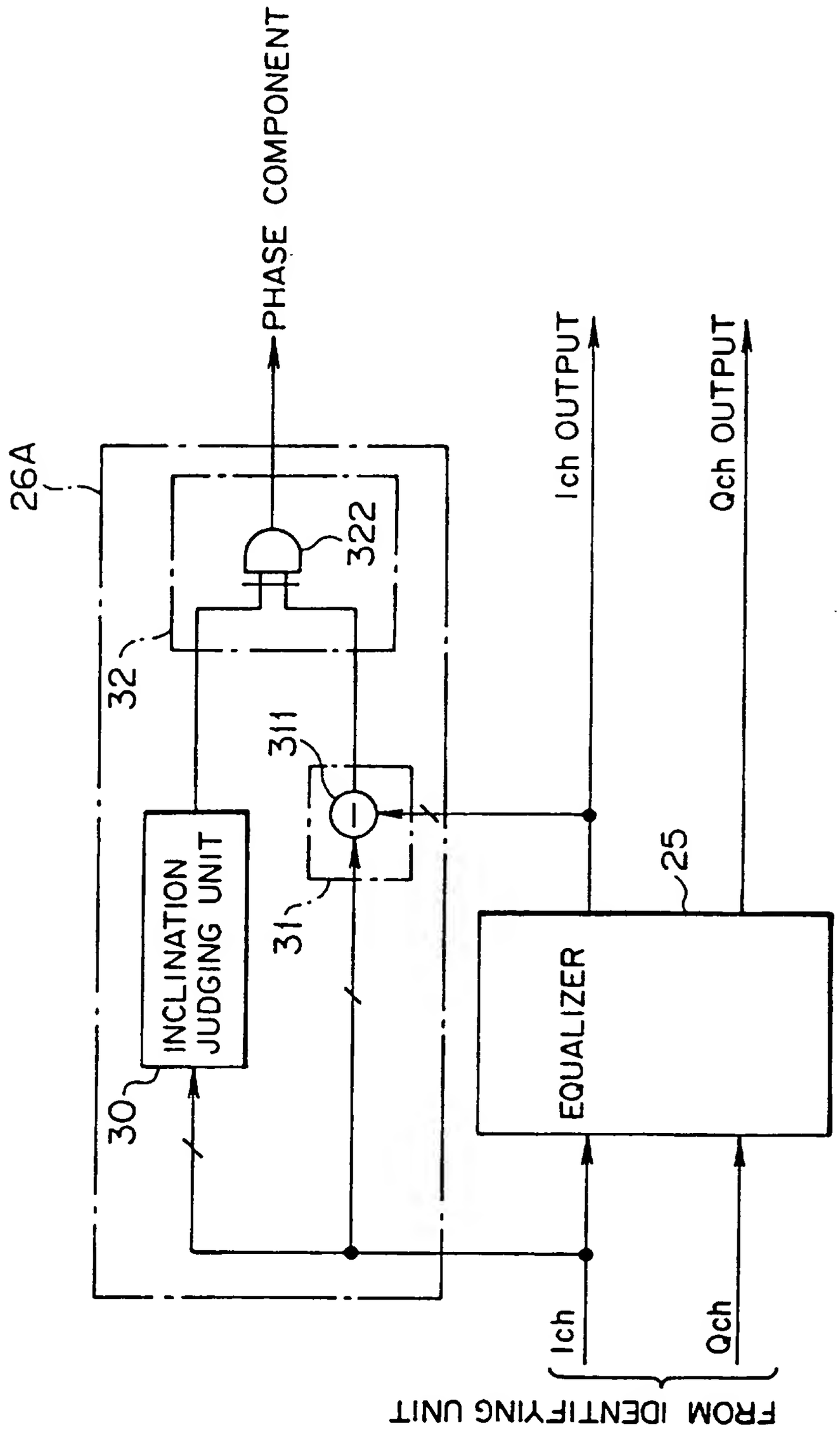

PHASE COMPONENT
26A
322
32
311
31
INCLINATION JUDGING UNIT
30
Ich OUTPUT
Qch OUTPUT
25
EQUALIZER
Ich
Qch
FROM IDENTIFYING UNIT

FIG. 12

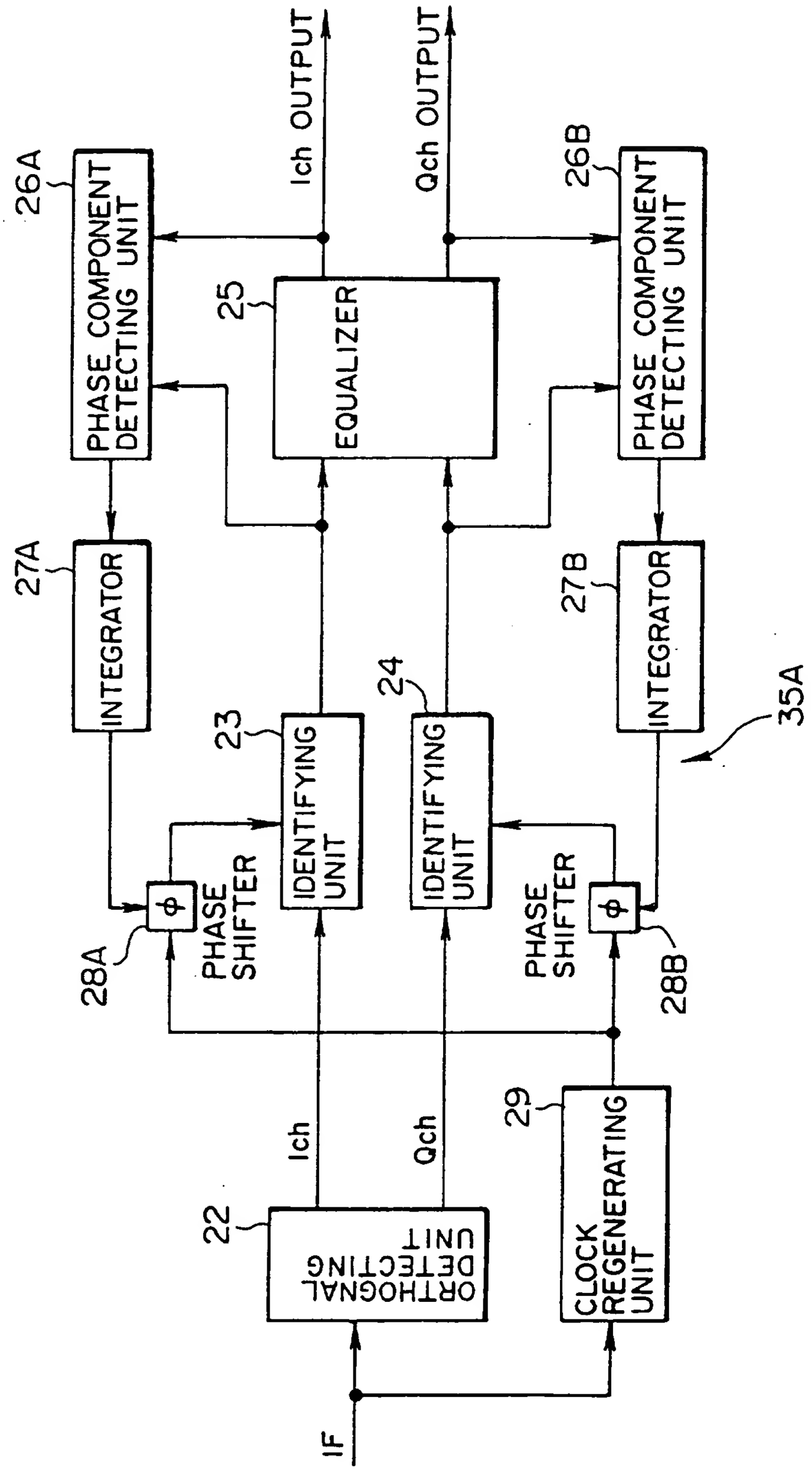

Ich OUTPUT
Qch OUTPUT
26A
26B
PHASE COMPONENT DETECTING UNIT
25
EQUALIZER
27A
27B
INTEGRATOR
23
24
IDENTIFYING UNIT
28A
28B
PHASE SHIFTER
35A
Ich
Qch
22
ORTHOGNAL DETECTING UNIT
29
CLOCK REGENERATING UNIT
IF

FIG. 13

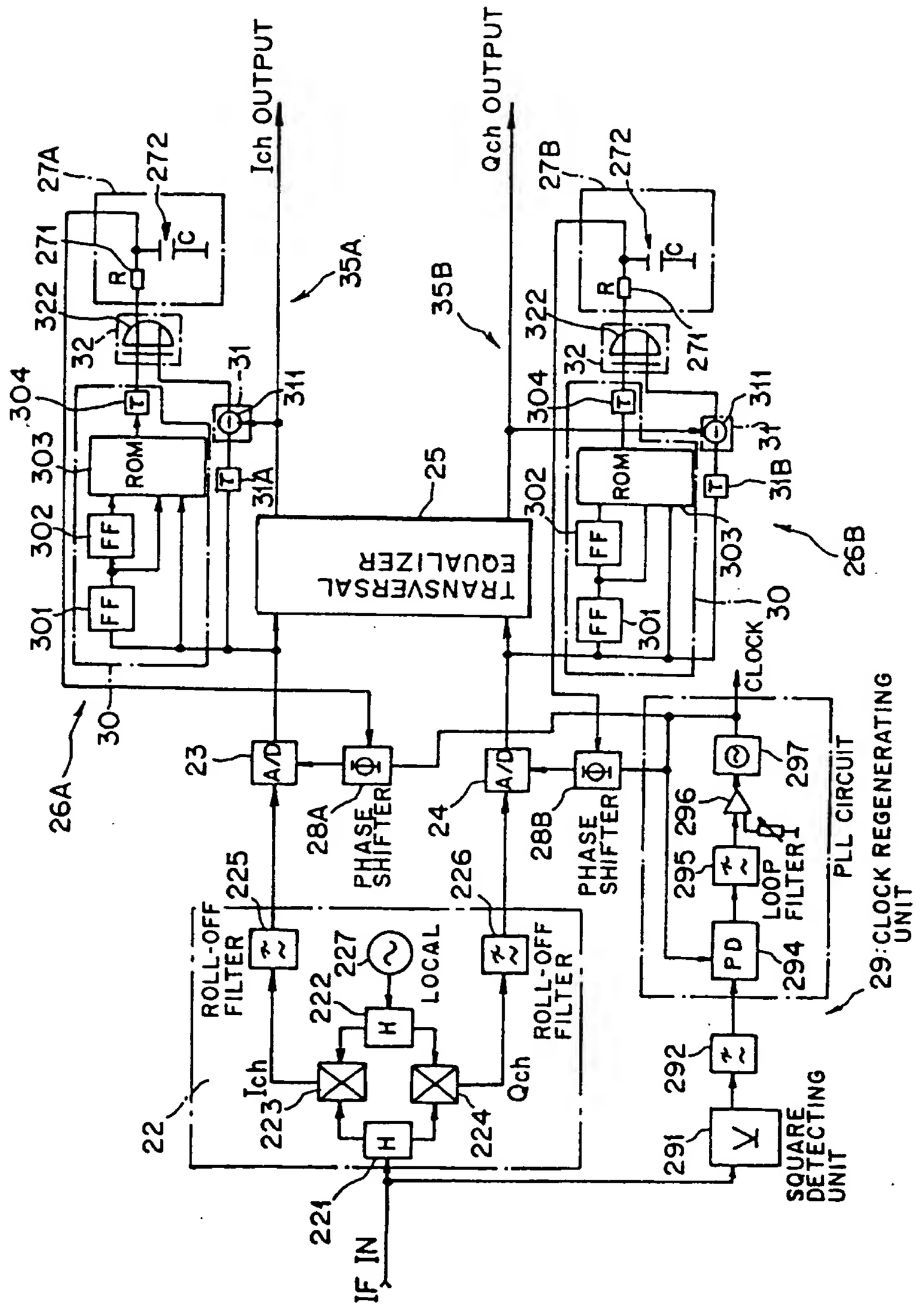


FIG. 14

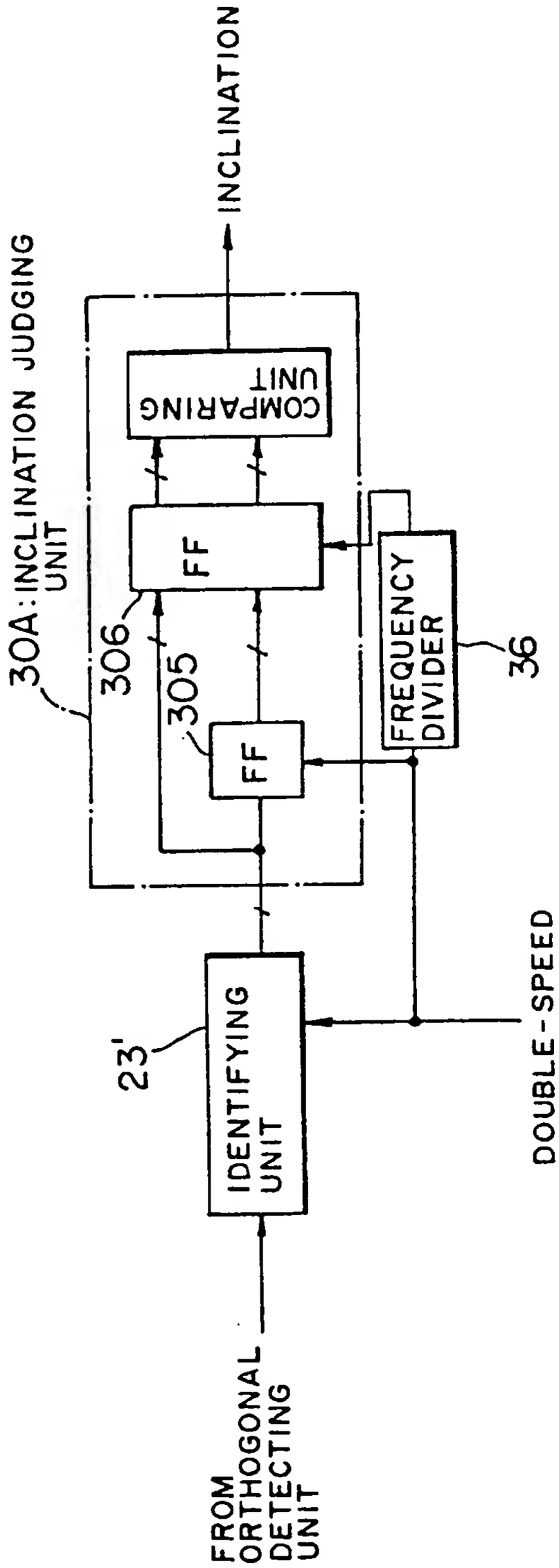

30A: INCLINATION JUDGING UNIT
COMPARING UNIT
FF
306
305
FF
FREQUENCY DIVIDER
36
23'
IDENTIFYING UNIT
FROM ORTHOGONAL DETECTING UNIT
DOUBLE-SPEED CLOCK

FIG. 15

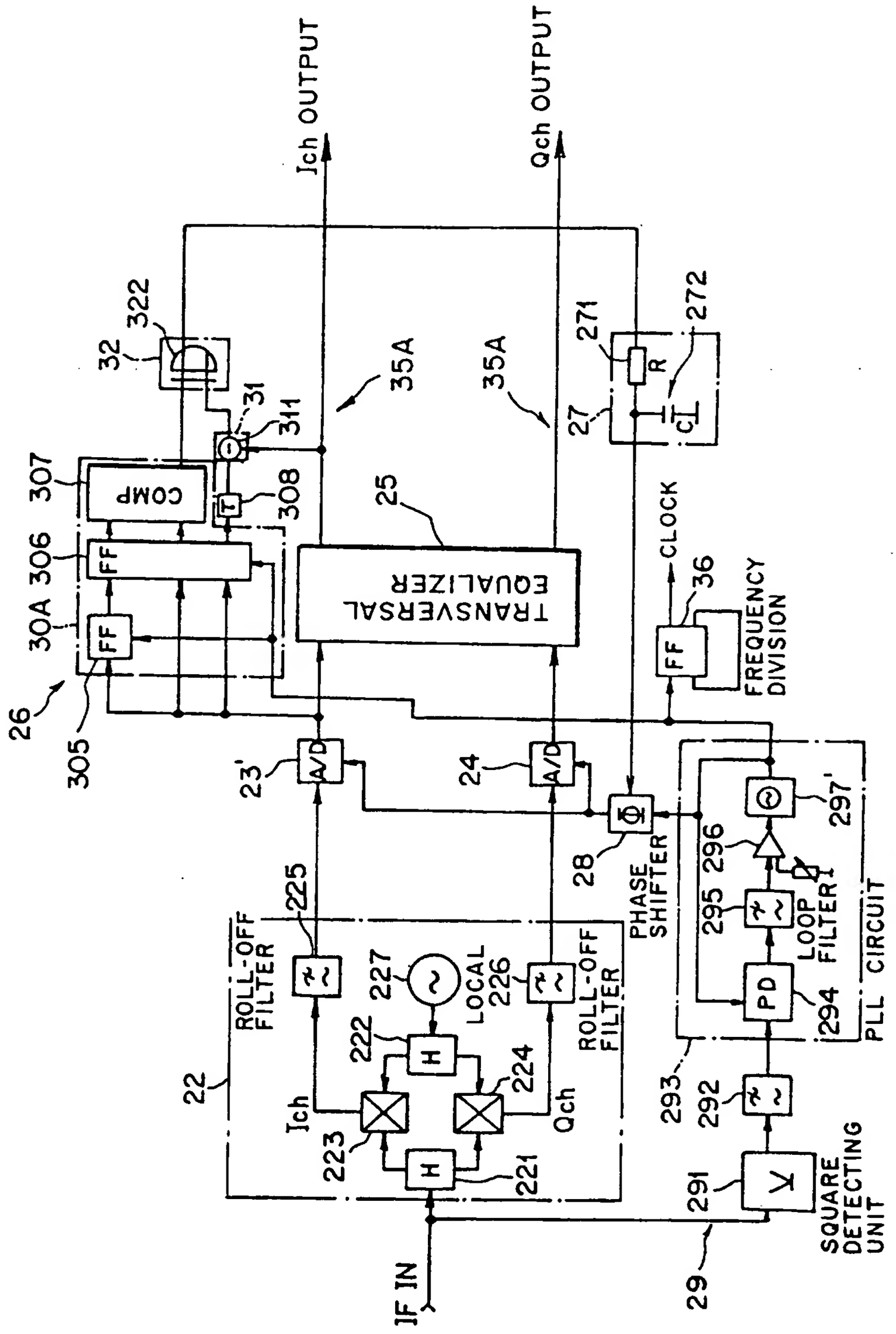

Ich OUTPUT
Qch OUTPUT
322
32
31
311
35A
35A
271
272
27
R
307
COMP
308
25
306
FF
30A
TRANSVERSAL EQUALIZER
CLOCK
36
FF
FREQUENCY DIVISION
26
305
23'
A/D
24
A/D
28
PHASE SHIFTER
297'
296
295
LOOP FILTER
PD
294
PLL CIRCUIT
225
ROLL-OFF FILTER
227
LOCAL
226
ROLL-OFF FILTER
222
224
22
Ich
Qch
223
221
293
292
291
SQUARE DETECTING UNIT
IF IN
29

FIG. 16

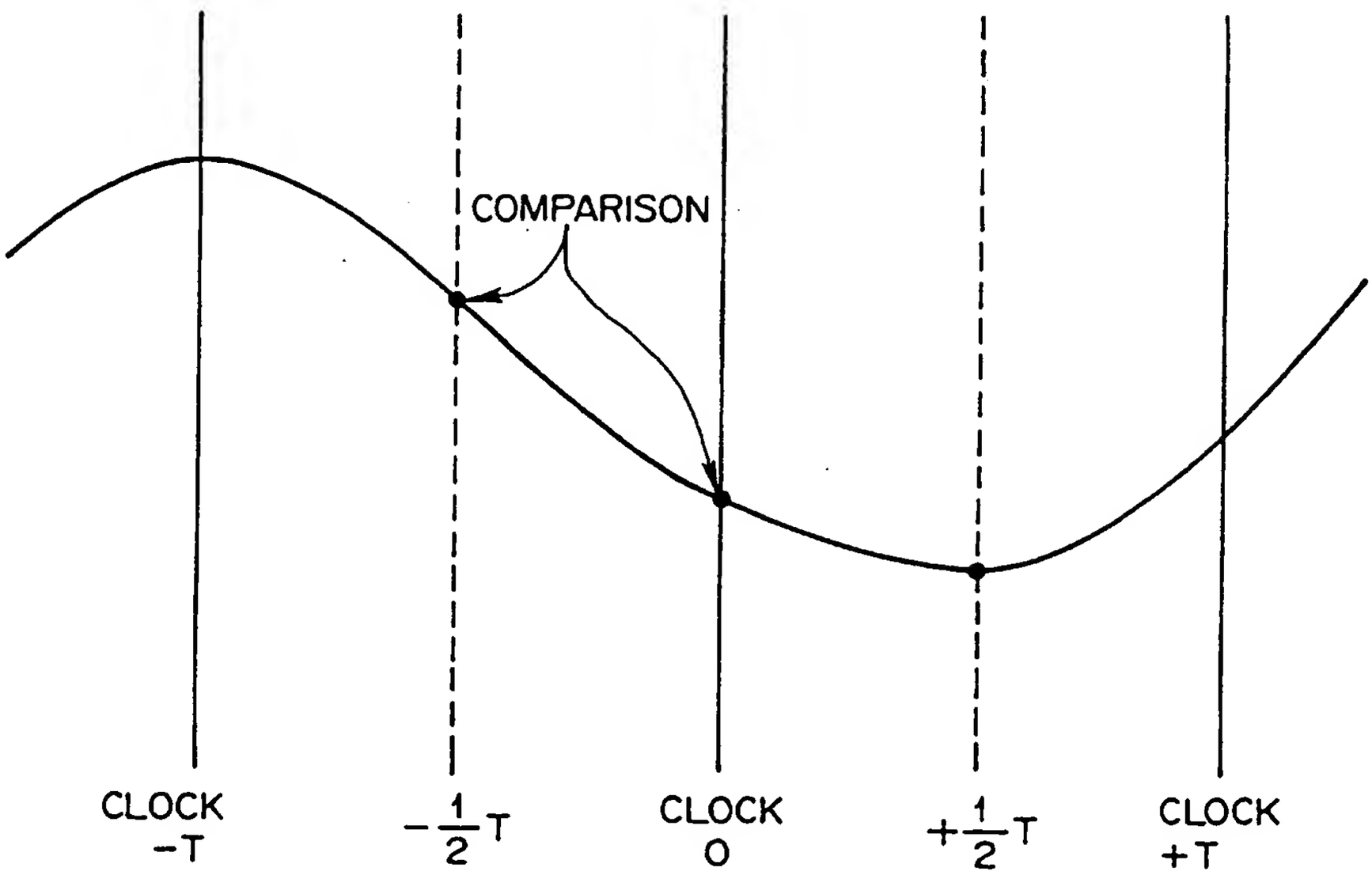


FIG. 17

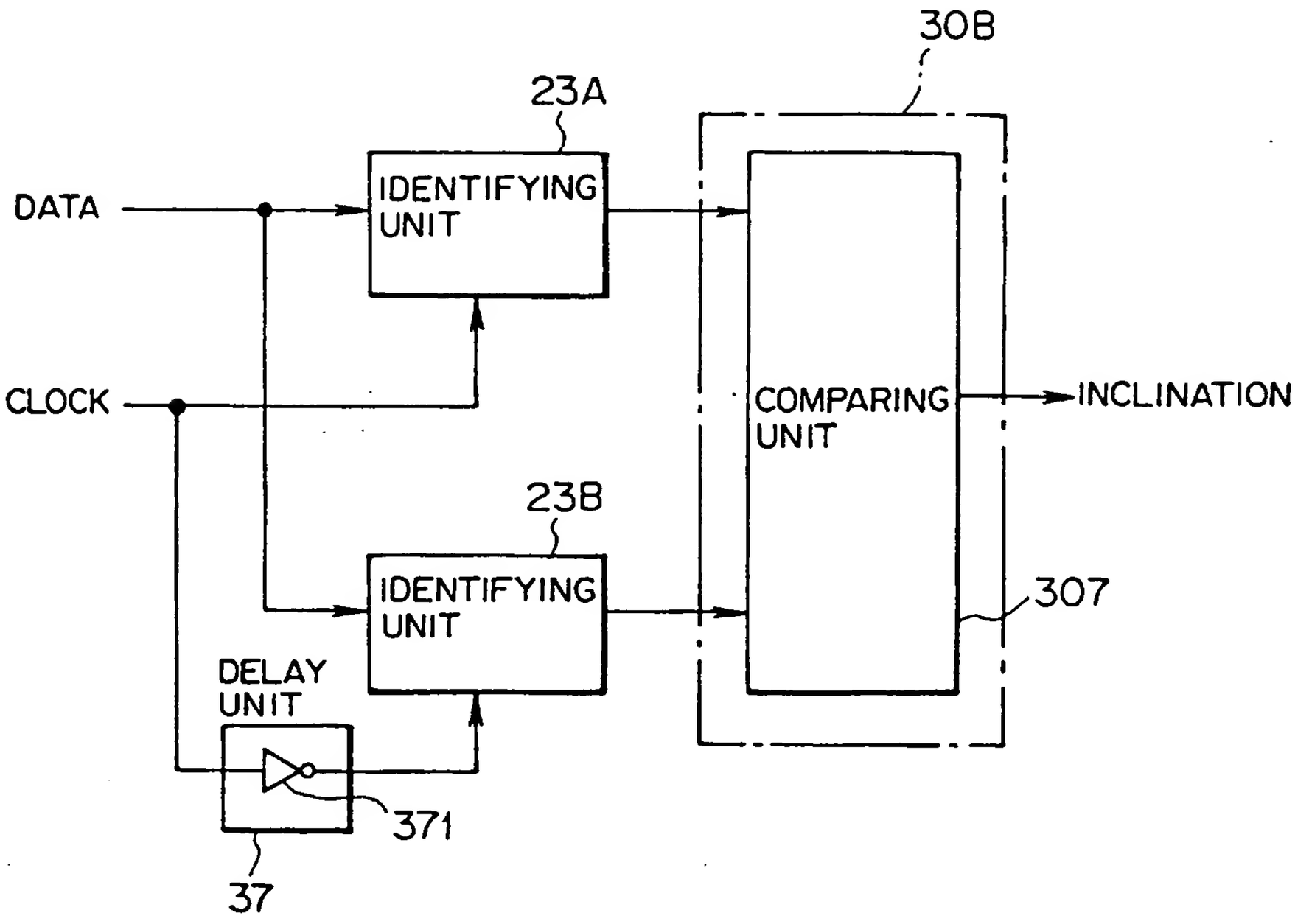
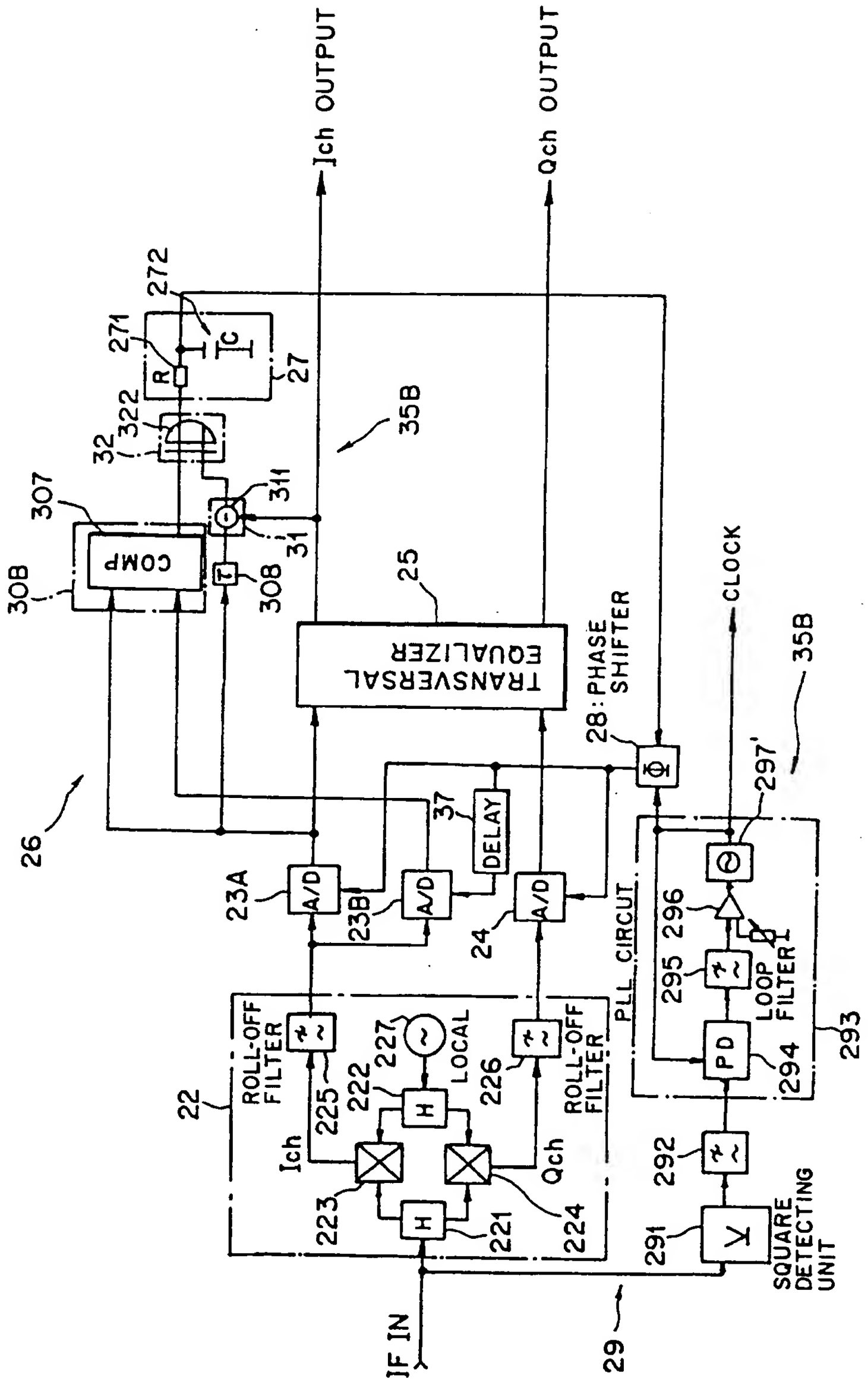

30B
23A
DATA
IDENTIFYING UNIT
CLOCK
COMPARING UNIT
INCLINATION
23B
IDENTIFYING UNIT
307
DELAY UNIT
371
37

FIG. 18


Ich OUTPUT
Qch OUTPUT
272
271
R
Ic
I
27
322
32
35B
307
311
COMP
308
31
25
TRANSVERSAL EQUALIZER
28: PHASE SHIFTER
CLOCK
26
37
DELAY
297'
23A
23B
24
A/D
PLL CIRCUIT
295
296
LOOP FILTER
PD
294
293
292
291
SQUARE DETECTING UNIT
ROLL-OFF FILTER
22
225
222
227
LOCAL
226
Ich
Qch
223
221
224
IF IN
29

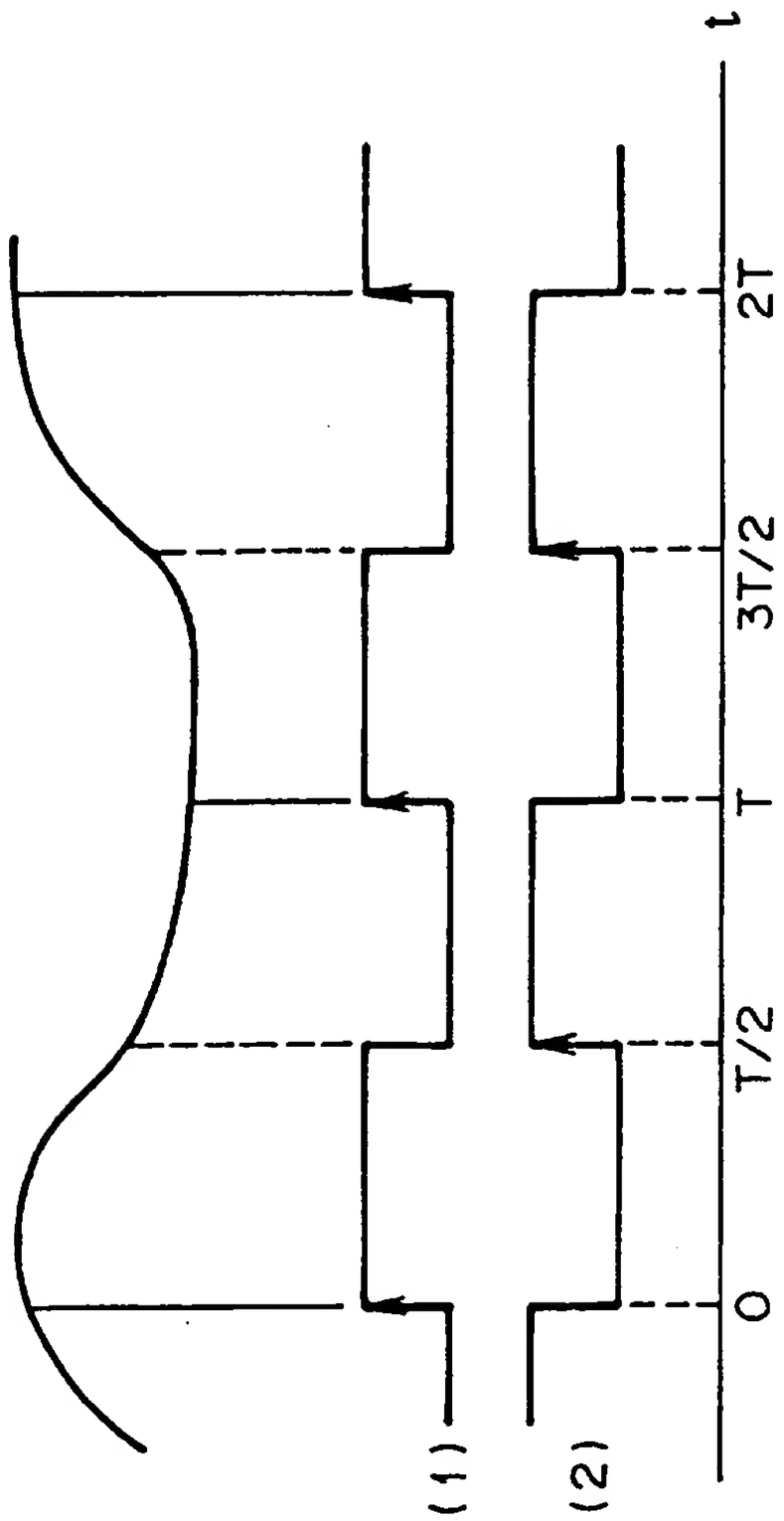


FIG.19(a)

FIG.19(b)

FIG.19(c)

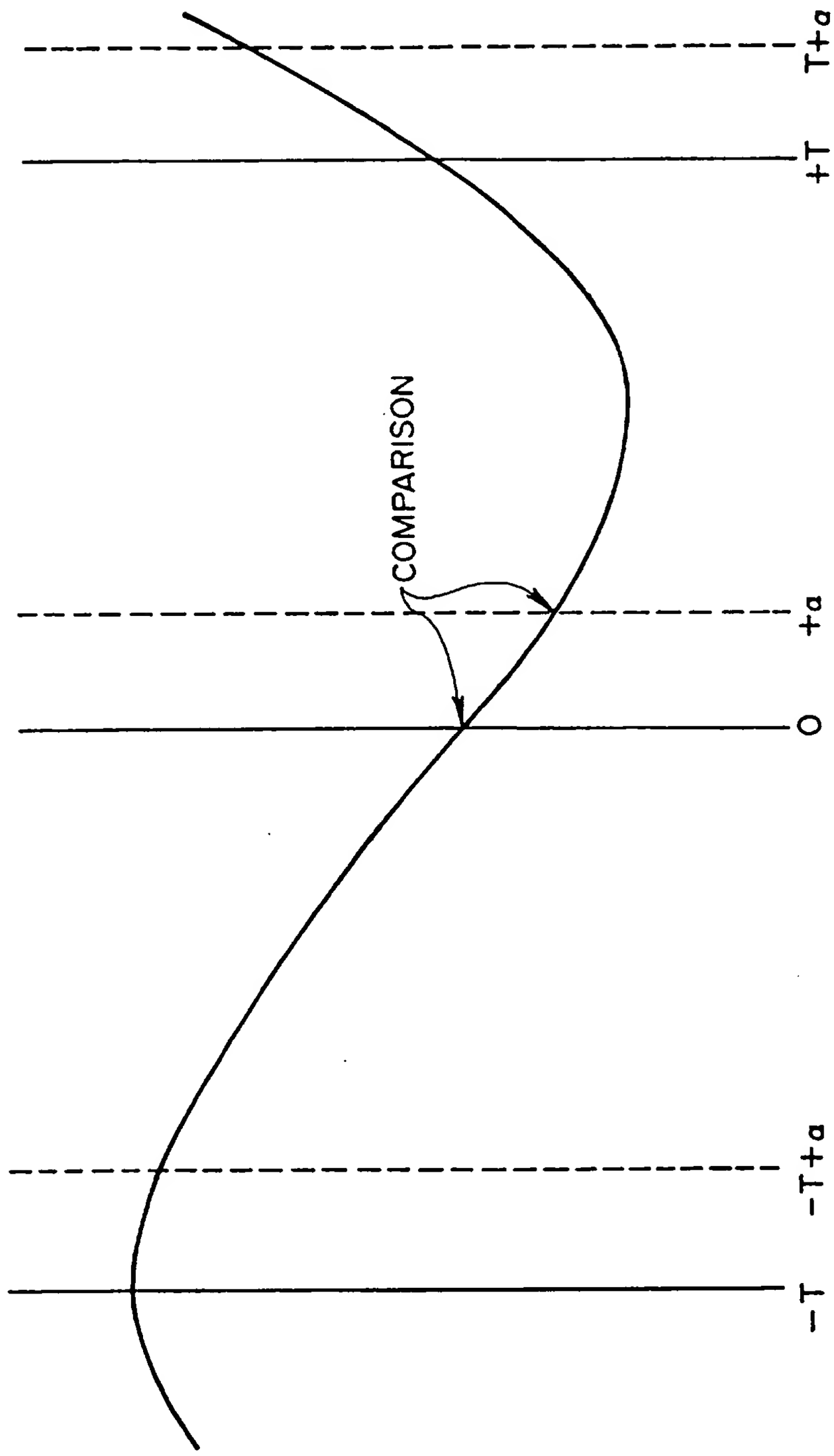


FIG. 20

FIG.21

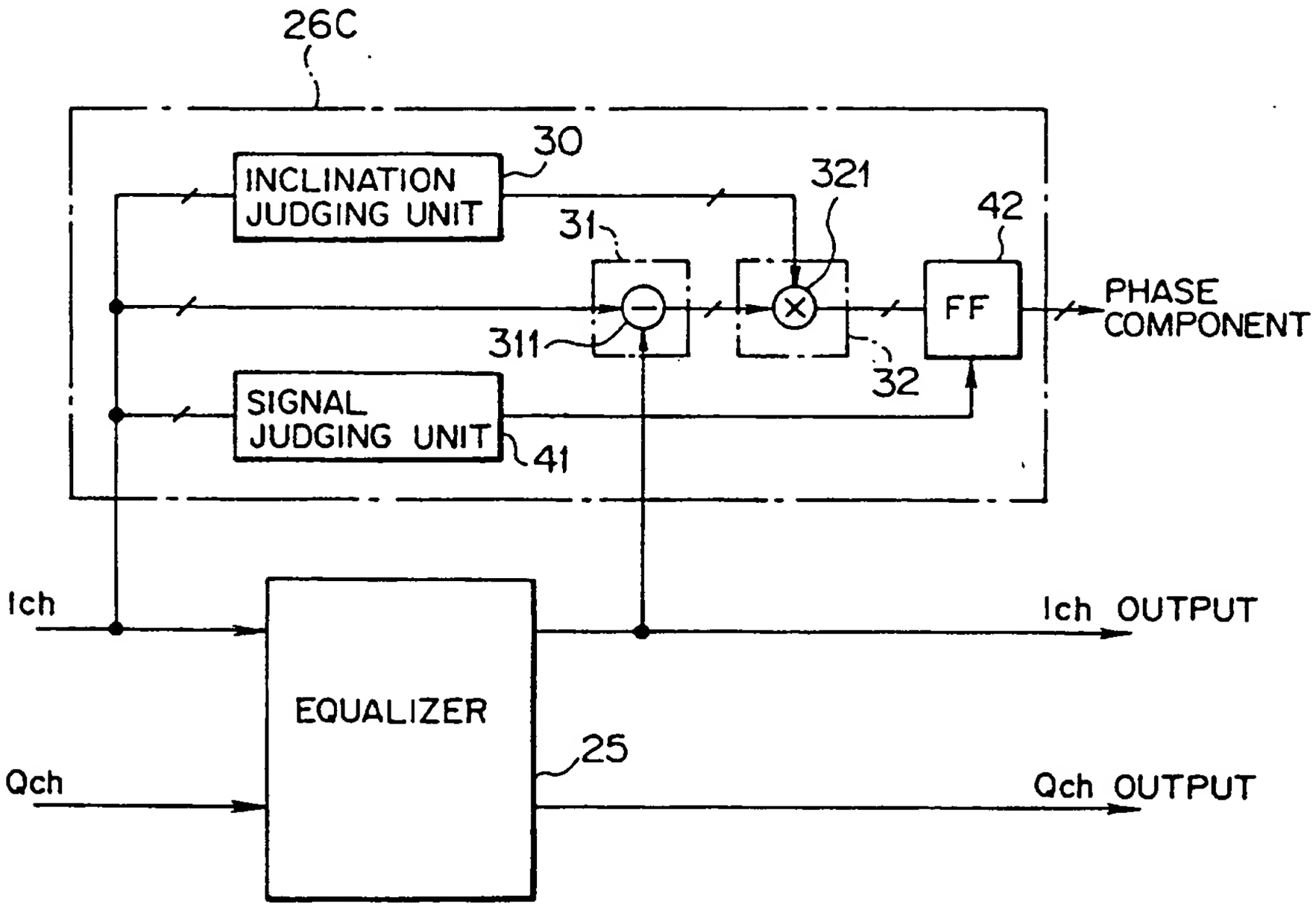

26C
30
INCLINATION JUDGING UNIT
321
31
42
FF
PHASE COMPONENT
311
32
SIGNAL JUDGING UNIT
41
Ich
Ich OUTPUT
EQUALIZER
25
Qch
Qch OUTPUT

FIG. 22

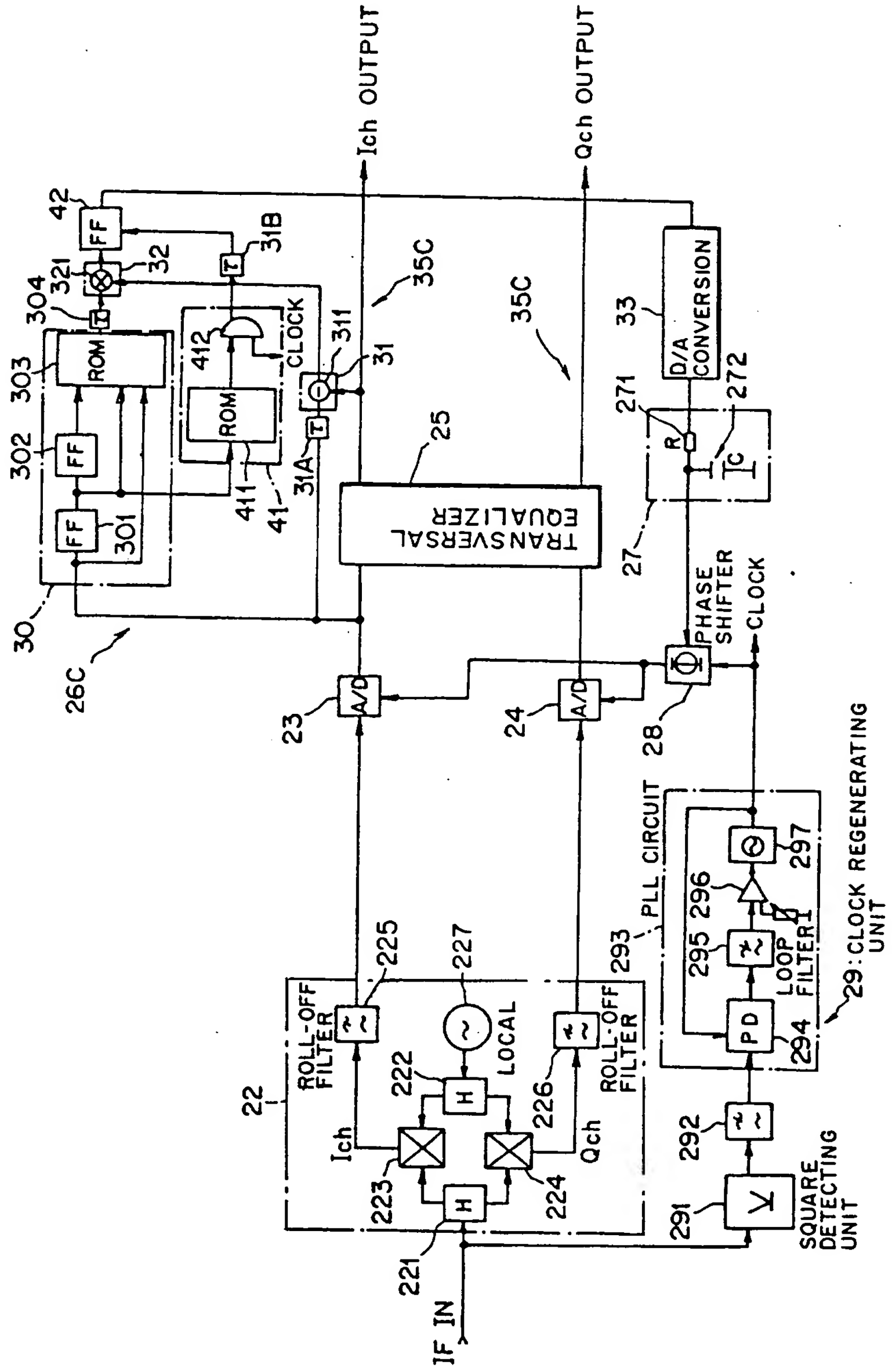
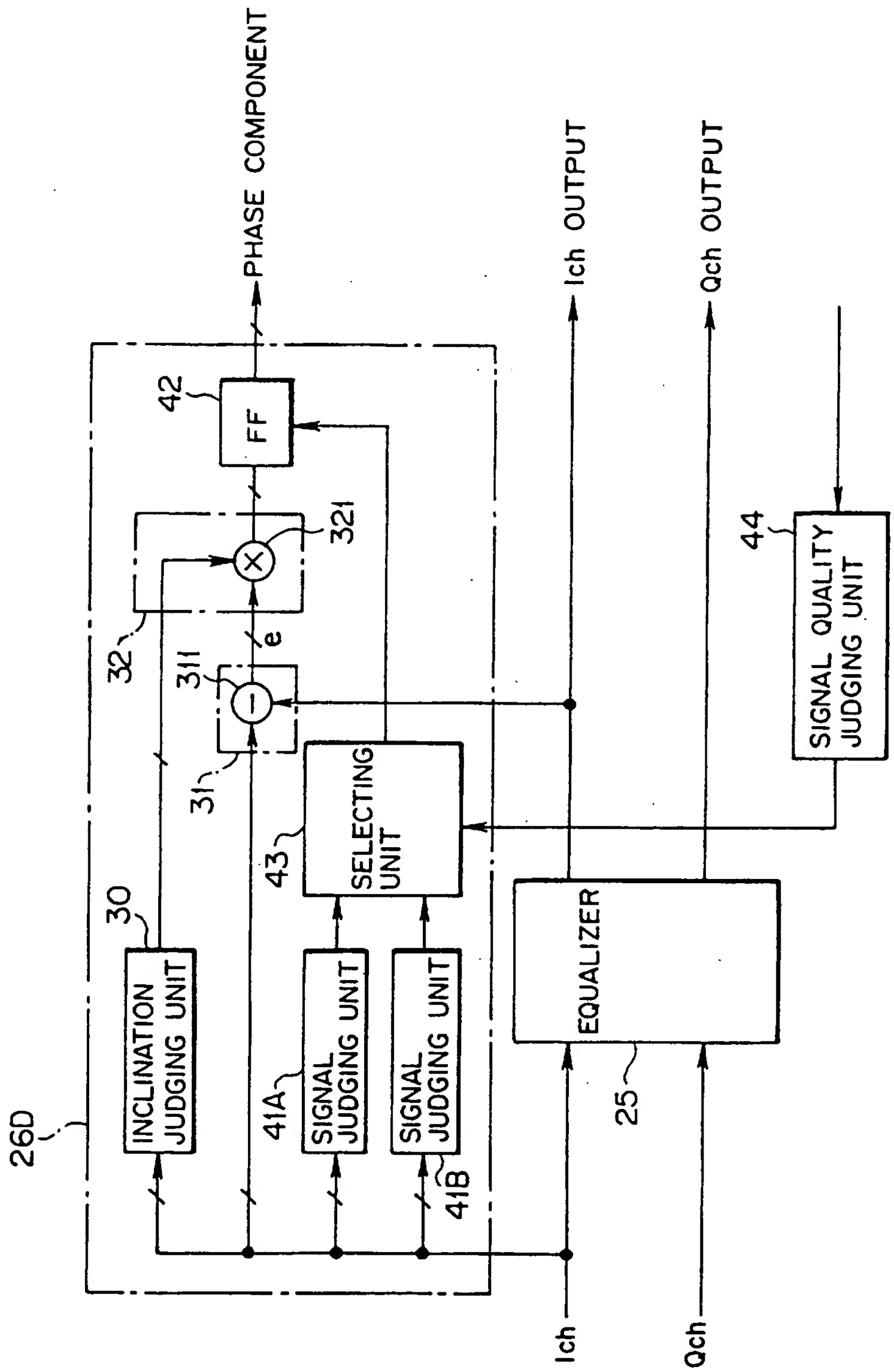

Ich OUTPUT
Qch OUTPUT
42
FF
32
318
304
321
303
ROM
412
CLOCK
311
31
35C
302
FF
301
411
41
31A
25
TRANSVERSAL EQUALIZER
271
272
R
Tc
27
D/A CONVERSION
33
30
26C
23
24
A/D
PHASE SHIFTER
CLOCK
28
PLL CIRCUIT
297
296
295
LOOP FILTER
PD
294
29: CLOCK REGENERATING UNIT
293
292
291
SQUARE DETECTING UNIT
22
ROLL-OFF FILTER
225
227
LOCAL
222
226
223
224
221
IF IN

FIG.23


PHASE COMPONENT
OUTPUT
OUTPUT
Ich
Qch
42
FF
321
32
311
e
31
43
SELECTING UNIT
30
INCLINATION JUDGING UNIT
41A
SIGNAL JUDGING UNIT
SIGNAL JUDGING UNIT
41B
26D
44
SIGNAL QUALITY JUDGING UNIT
EQUALIZER
25
Ich
Qch

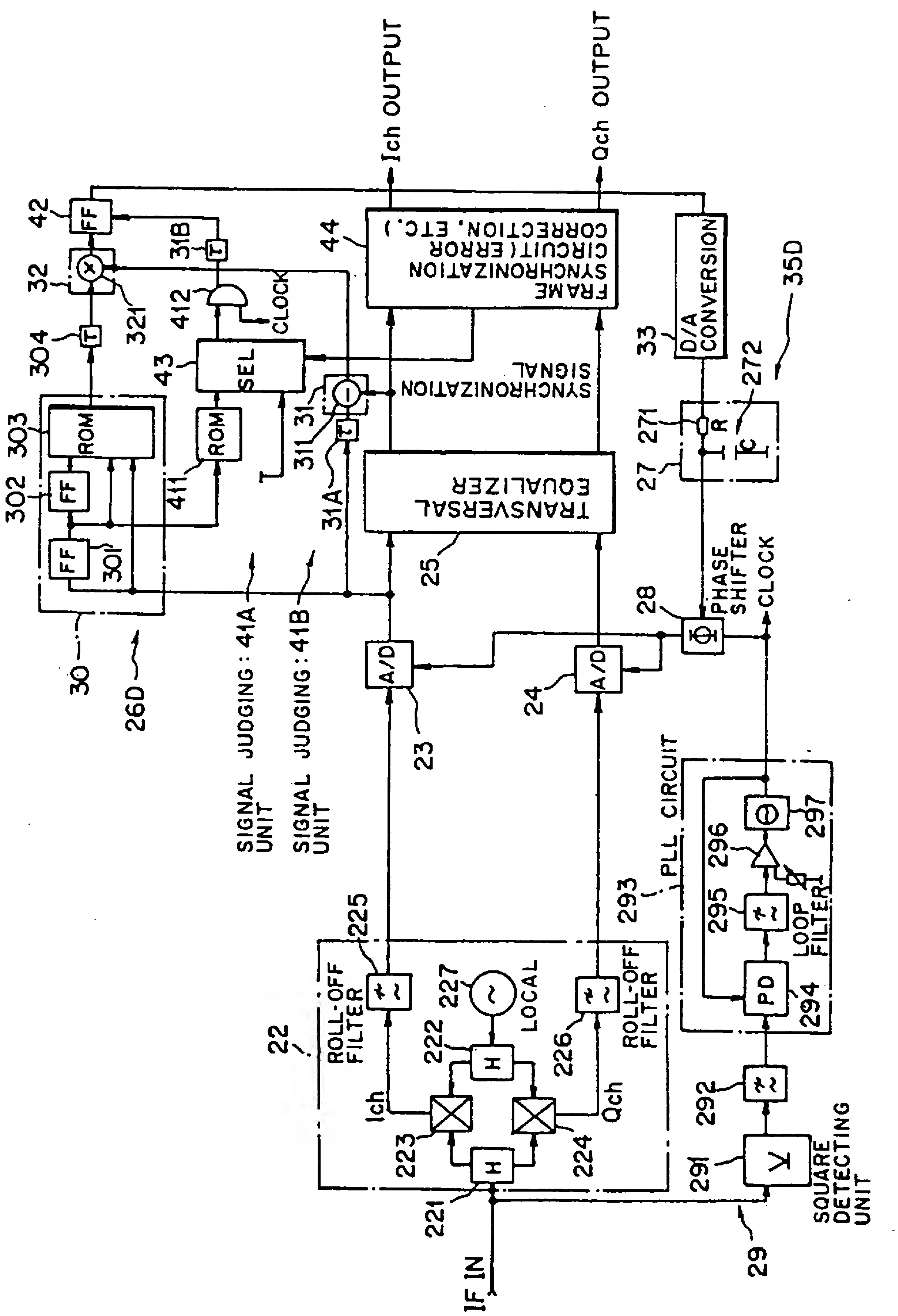

Ich OUTPUT
Qch OUTPUT
42
FF
32
321
304
31B
412
CLOCK
44
FRAME SYNCHRONIZATION CIRCUIT (ERROR CORRECTION, ETC.)
D/A CONVERSION
33
35D
43
SEL
303
ROM
302
FF
301
411
ROM
311 31
31A
SYNCHRONIZATION SIGNAL
271
R
272
C
27
TRANSVERSAL EQUALIZER
25
30
26D
SIGNAL JUDGING UNIT : 41A
SIGNAL JUDGING UNIT : 41B
28
PHASE SHIFTER
CLOCK
A/D
23
A/D
24
PLL CIRCUIT
293
297
296
295
LOOP FILTER
PD
294
225
ROLL-OFF FILTER
22
227
LOCAL
222
H
Ich
223
H
224
Qch
226
ROLL-OFF FILTER
221
IF IN
292
291
SQUARE DETECTING UNIT
29

FIG. 24

FIG. 25

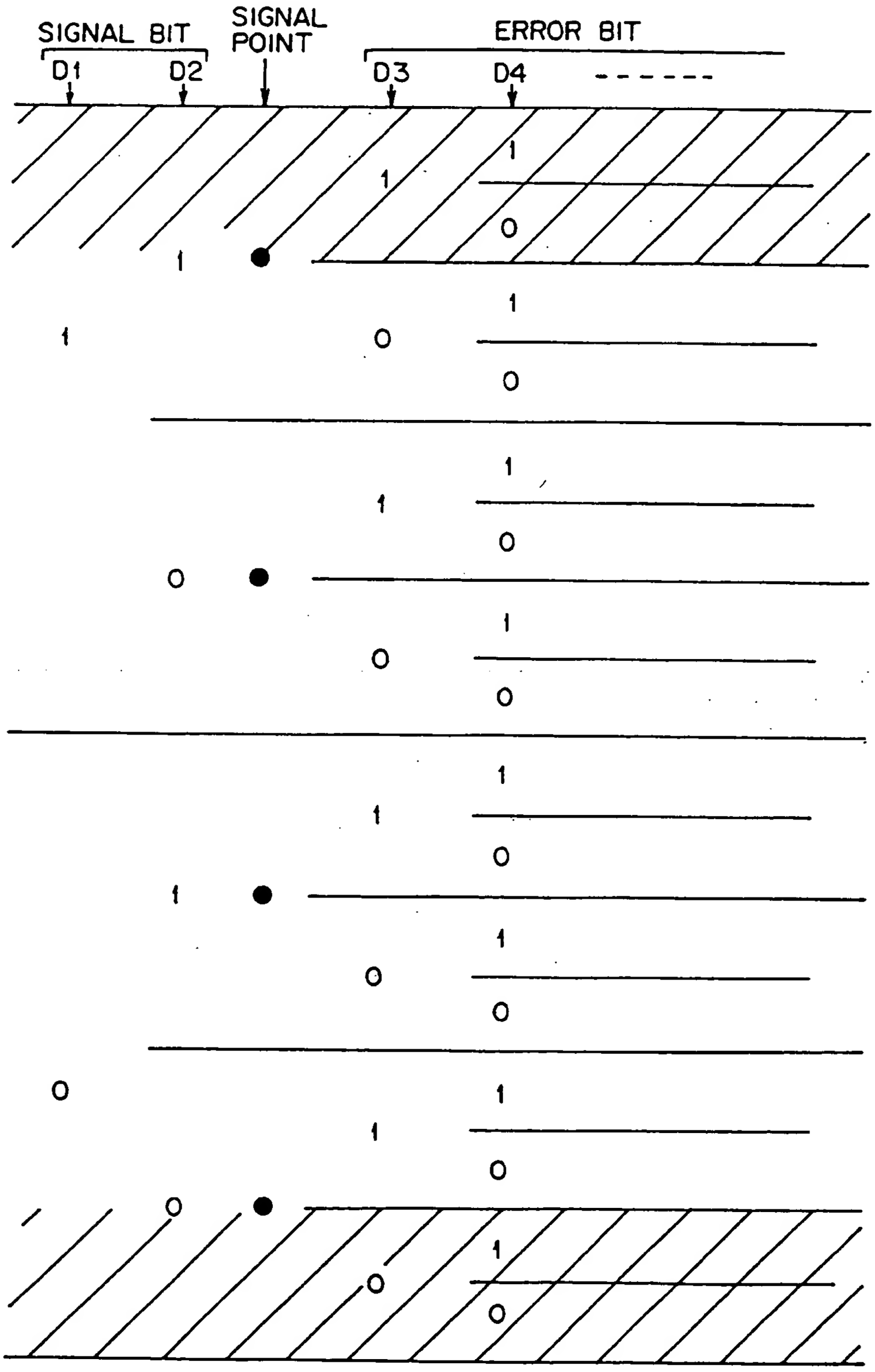


FIG.26

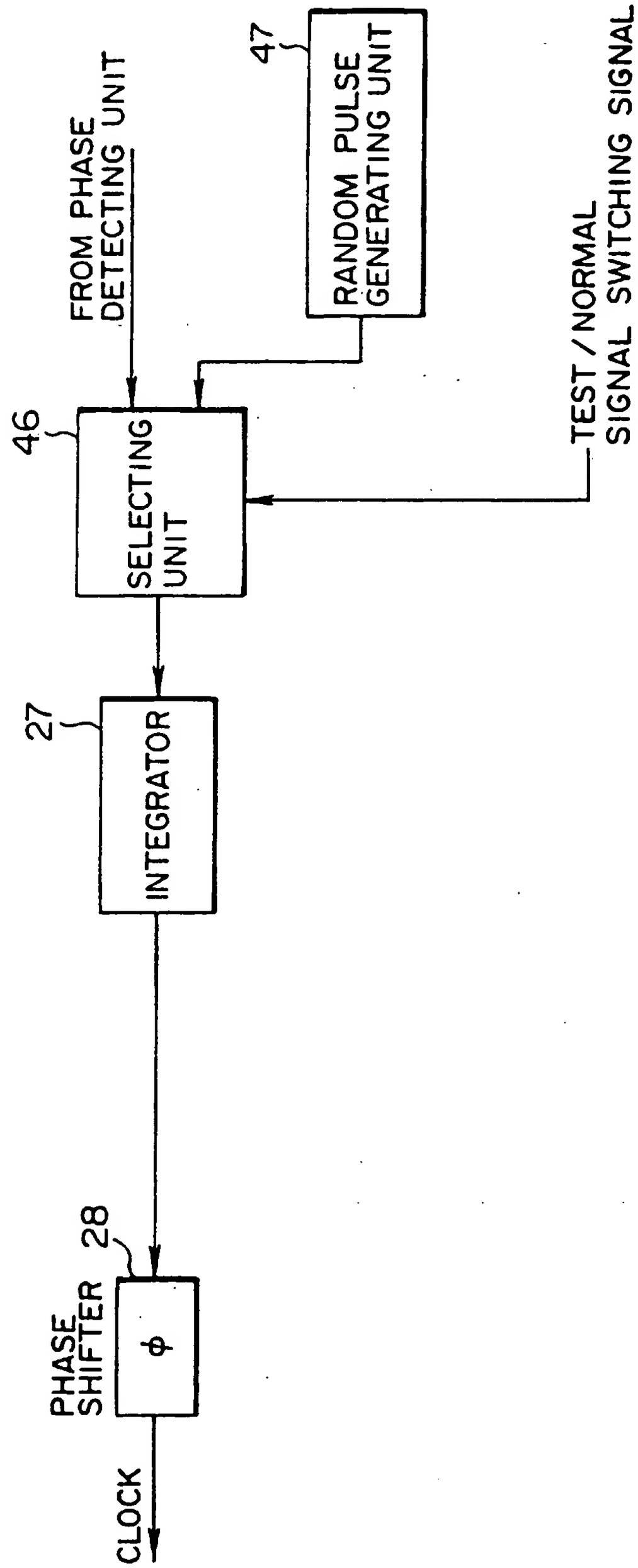

FROM PHASE DETECTING UNIT
47
RANDOM PULSE GENERATING UNIT
TEST/NORMAL SIGNAL SWITCHING SIGNAL
46
SELECTING UNIT
27
INTEGRATOR
28
PHASE SHIFTER
φ
CLOCK

FIG. 27

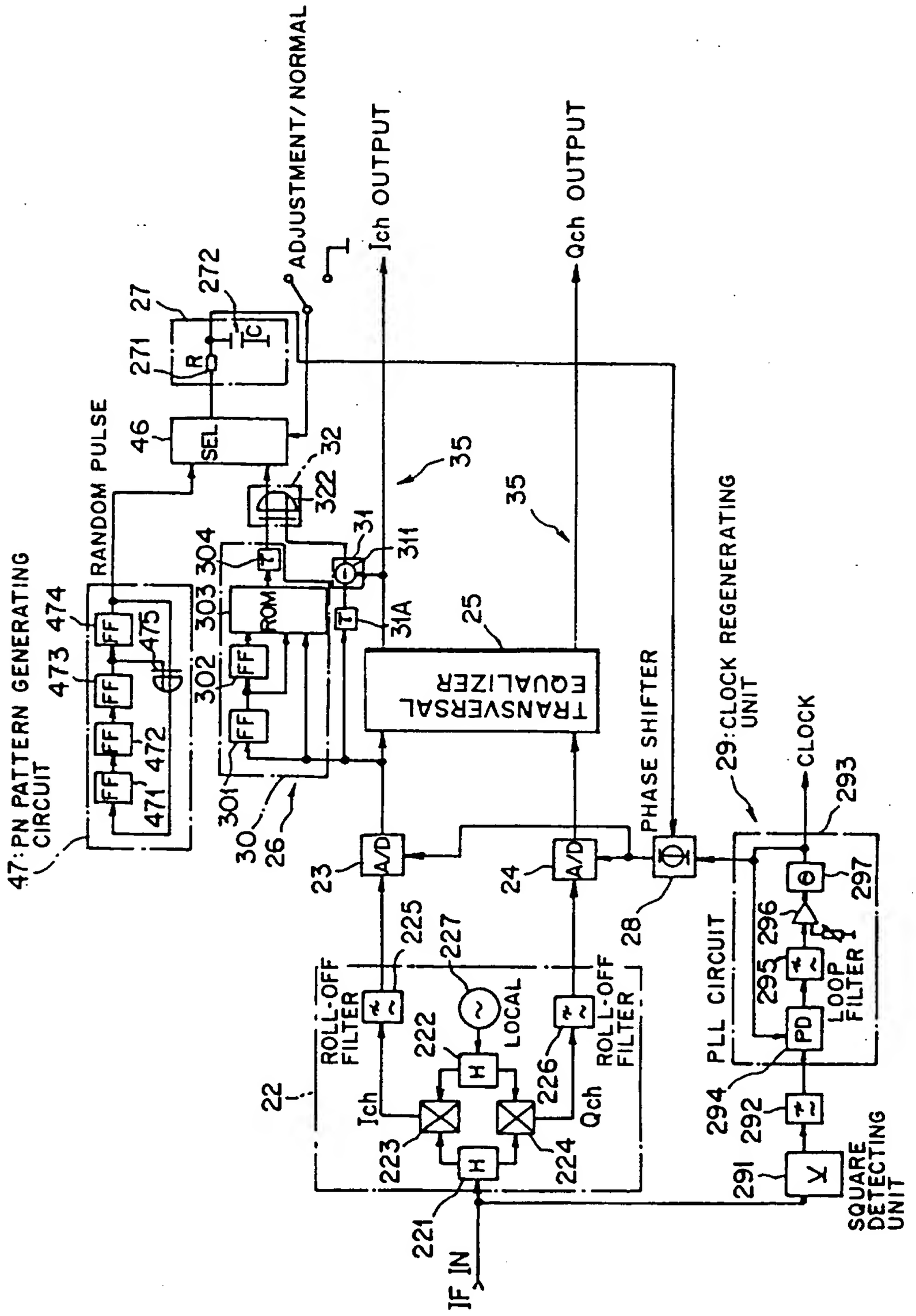

47: PN PATTERN GENERATING CIRCUIT
RANDOM PULSE
ADJUSTMENT/ NORMAL
Ich OUTPUT
Qch OUTPUT
TRANSVERSAL EQUALIZER
PHASE SHIFTER
29: CLOCK REGENERATING UNIT
CLOCK
PLL CIRCUIT
LOOP FILTER
SQUARE DETECTING UNIT
ROLL-OFF FILTER
LOCAL
IF IN
ROM
FF
SEL
A/D
PD

FIG.28

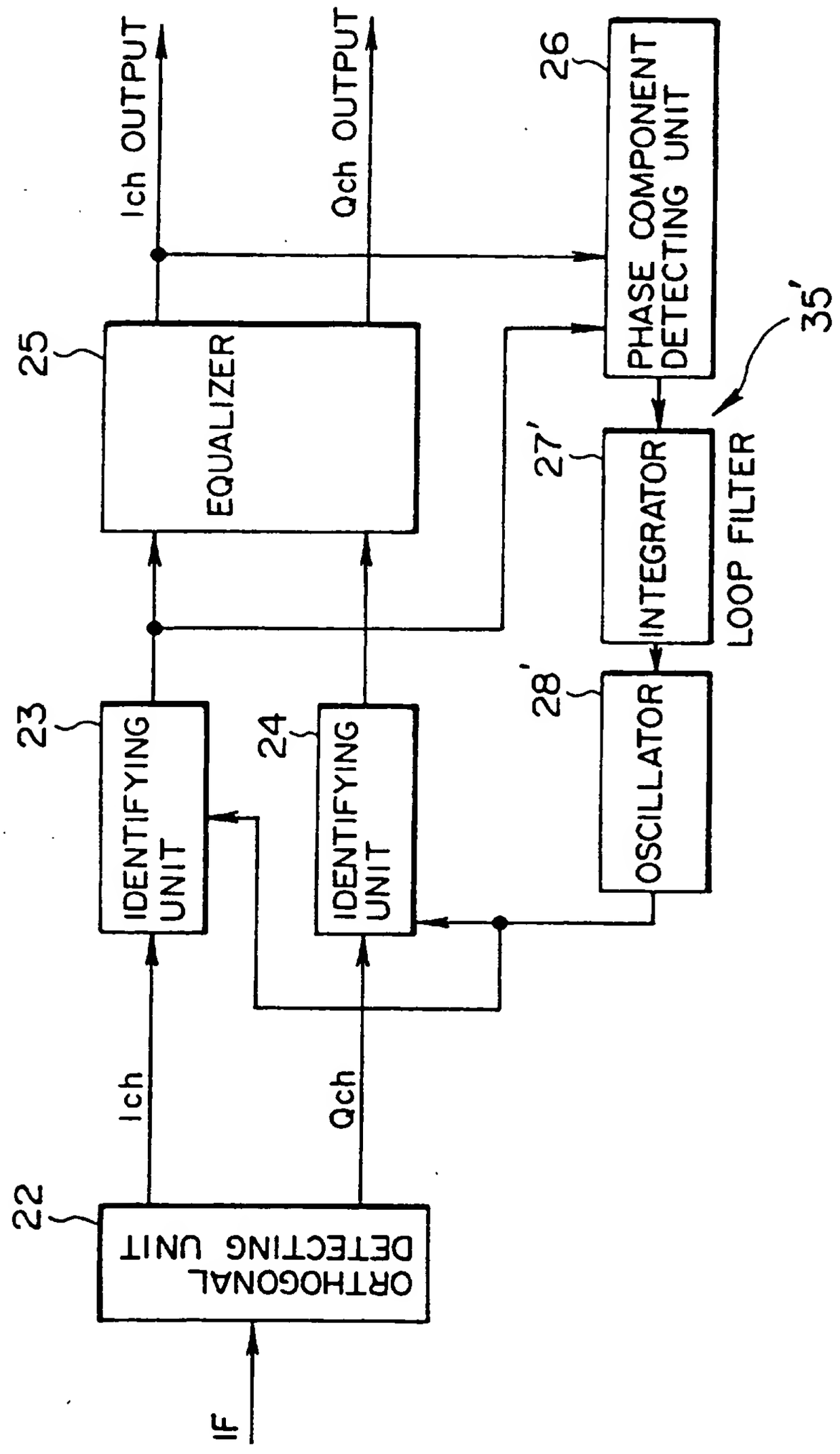

IF
ORTHOGONAL DETECTING UNIT
22
Ich
Qch
IDENTIFYING UNIT
23
IDENTIFYING UNIT
24
EQUALIZER
25
26
PHASE COMPONENT DETECTING UNIT
OSCILLATOR
28'
INTEGRATOR
27'
LOOP FILTER
35'
Ich OUTPUT
Qch OUTPUT

FIG. 29

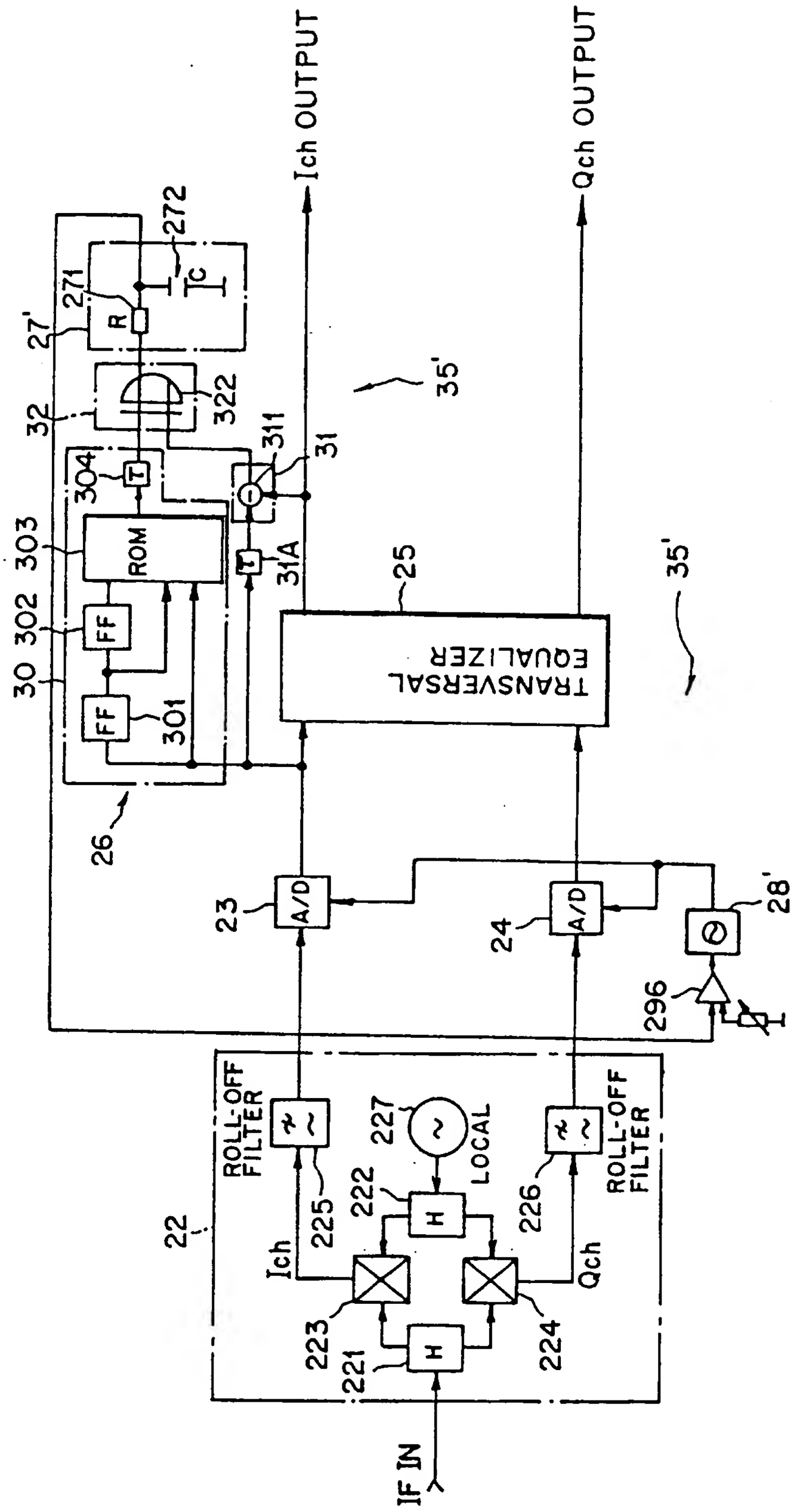

Ich OUTPUT
Qch OUTPUT
35'
272
271
27'
R
Tc
32
322
311
31
304
T
303
ROM
31A
30
302
FF
301
25
TRANSVERSAL EQUALIZER
26
23
24
A/D
28'
296
ROLL-OFF FILTER
227
LOCAL
222
225
226
22
Ich
Qch
223
224
221
H
IF IN

FIG. 30

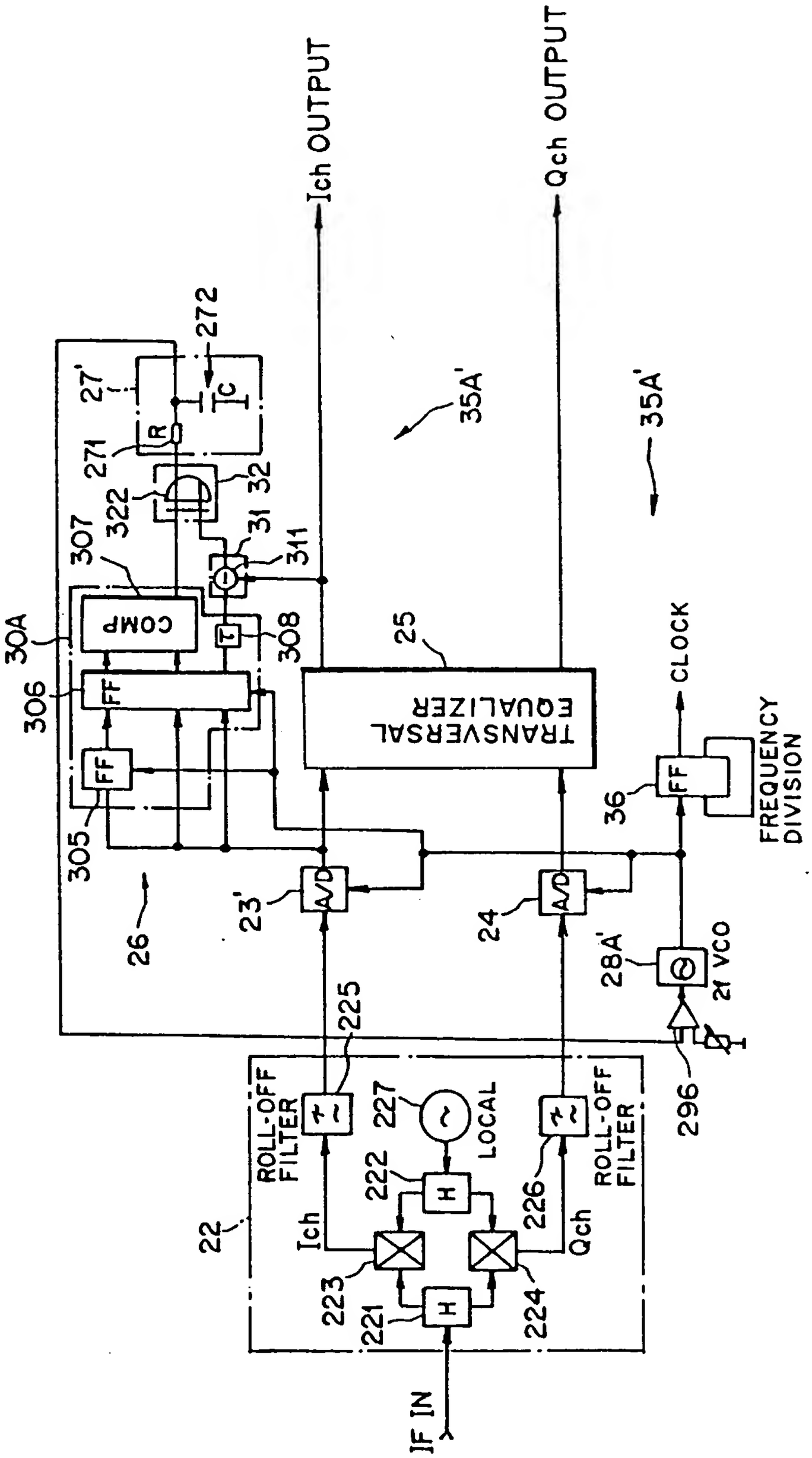

Ich OUTPUT
Qch OUTPUT
35A'
35A'
272
27
27'
271
R
Ic
32
322
31
311
307
COMP
308
30A
306
FF
FF
305
25
TRANSVERSAL EQUALIZER
CLOCK
36
FF
FREQUENCY DIVISION
26
23'
A/D
24
A/D
28A'
VCO
21
225
296
ROLL-OFF FILTER
ROLL-OFF FILTER
227
LOCAL
222
H
226
22
Ich
Qch
223
224
221
H
IF IN

FIG. 31

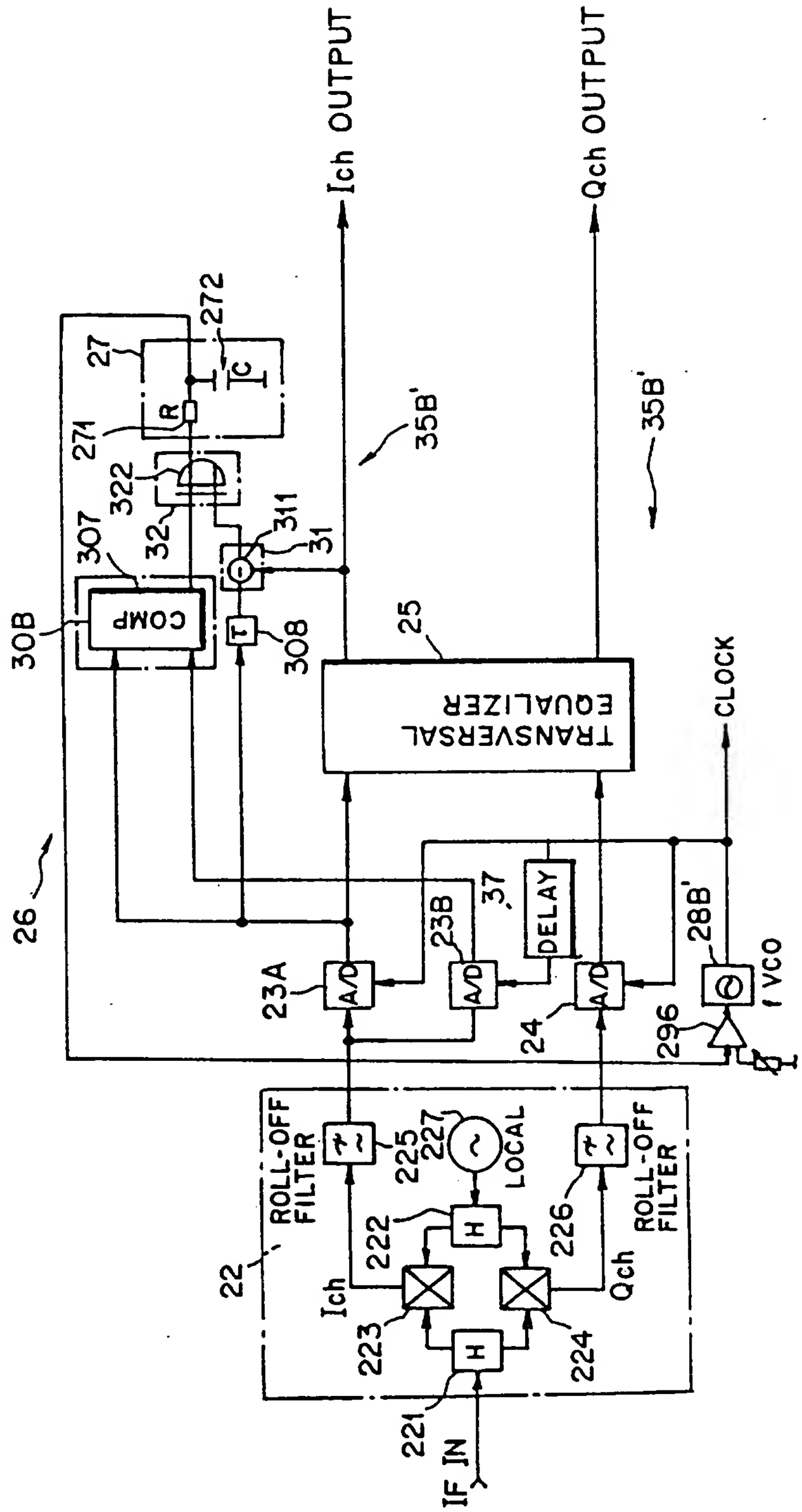

Ich OUTPUT
Qch OUTPUT
35B'
35B'
272
27
Ic
I
271
R
322
32
307
311
31
30B
COMP
T
308
25
TRANSVERSAL EQUALIZER
CLOCK
26
37
DELAY
23B
28B'
23A
A/D
24
296
f VCO
ROLL-OFF FILTER
ROLL-OFF FILTER
22
225
227
LOCAL
222
226
Ich
Qch
223
224
221
IF IN

FIG. 32

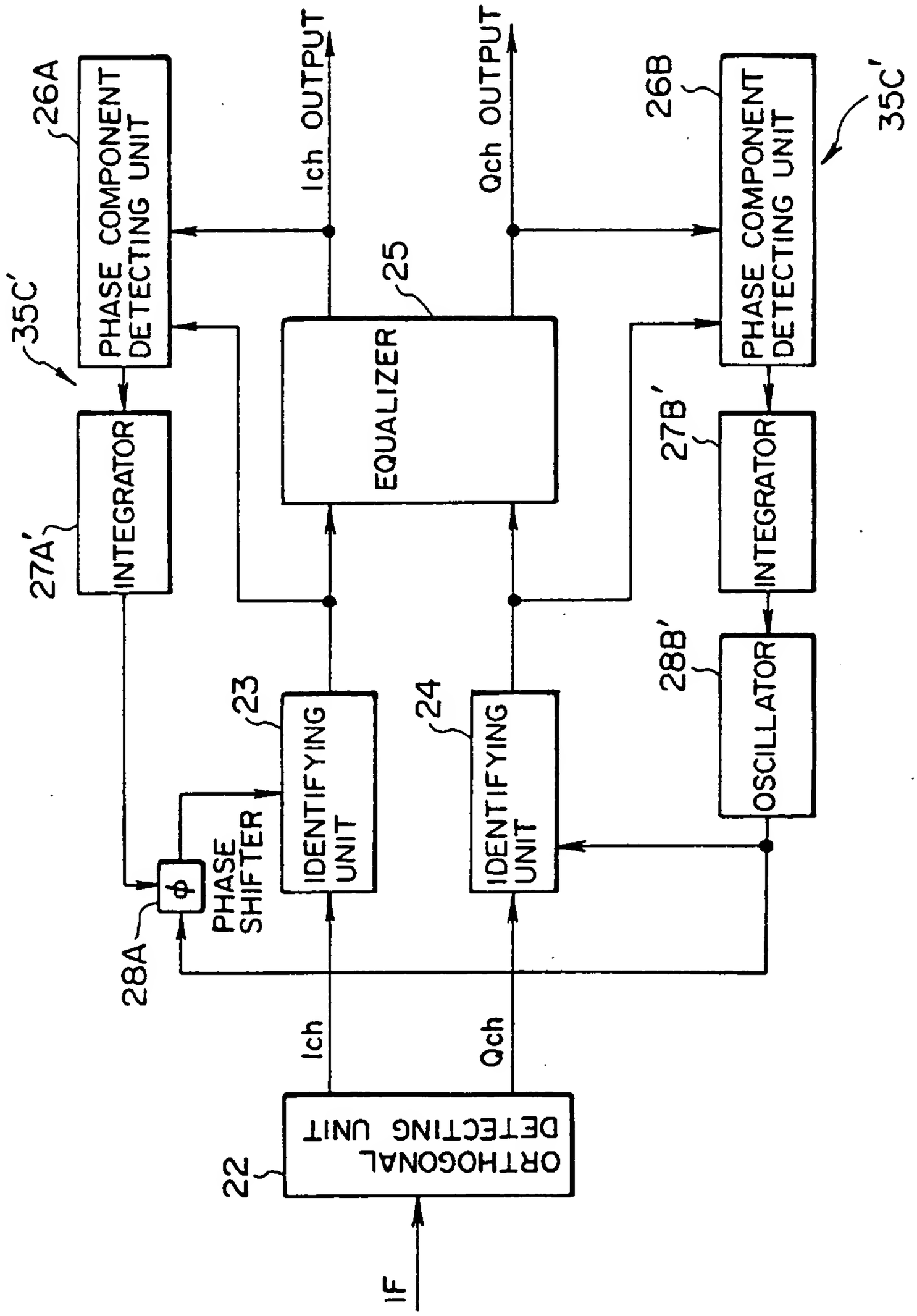

ORTHOGONAL DETECTING UNIT
22
Ich
Qch
IF
IDENTIFYING UNIT
23
IDENTIFYING UNIT
24
PHASE SHIFTER
φ
28A
INTEGRATOR
27A'
OSCILLATOR
28B'
INTEGRATOR
27B'
EQUALIZER
25
PHASE DETECTOR
35C'
PHASE DETECTOR
35C'
26A
26B
Ich OUTPUT
Qch OUTPUT

FIG. 33

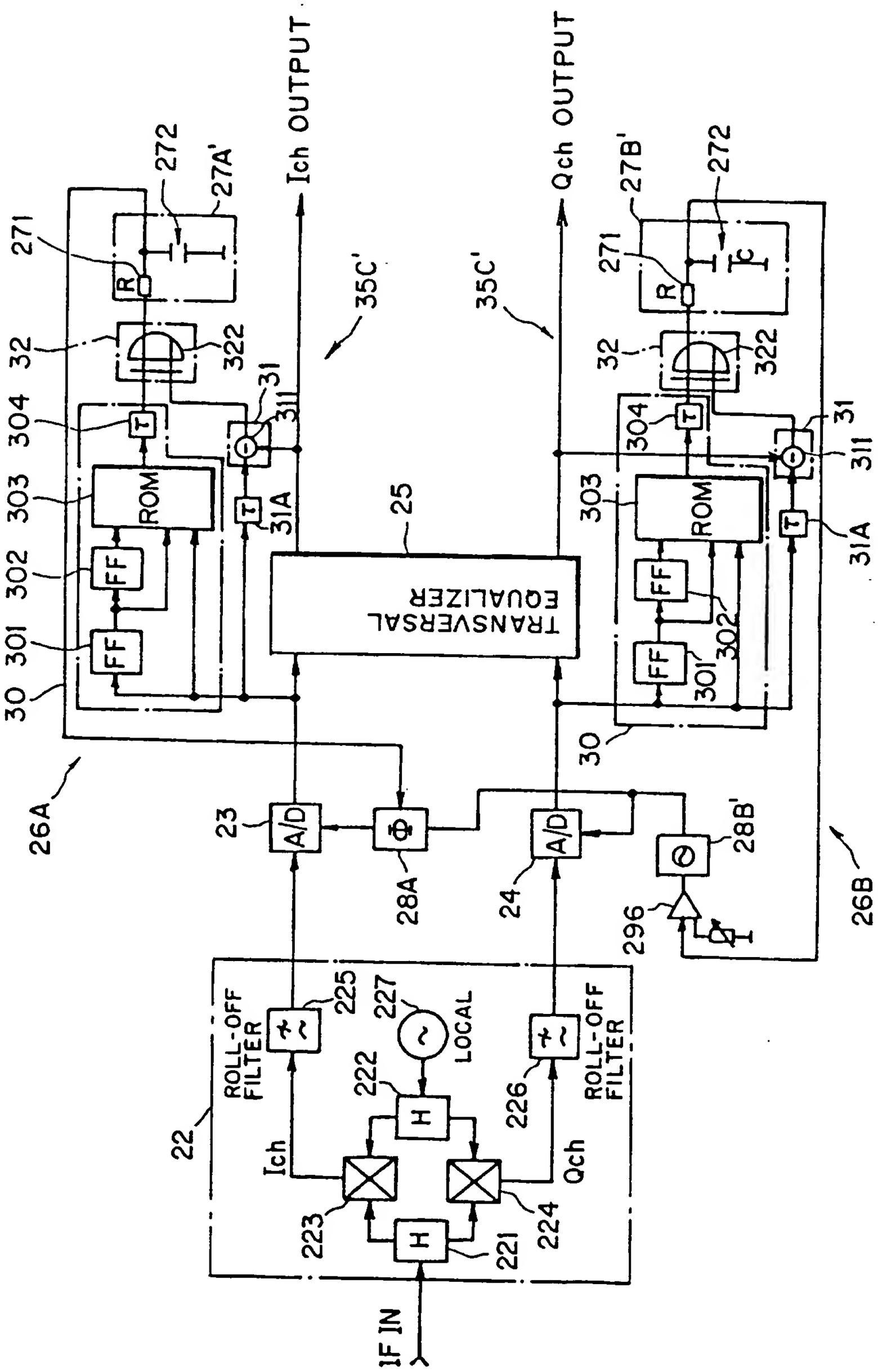

Ich OUTPUT
Qch OUTPUT
271
272
27A'
27B'
R
I
F
32
322
304
T
303
ROM
302
FF
301
30
31
311
31A
35C'
25
TRANSVERSAL EQUALIZER
26A
26B
23
24
A/D
Φ
28A
28B'
296
22
ROLL-OFF FILTER
225
227
LOCAL
222
226
H
223
224
221
Ich
Qch
IF IN

FIG. 34

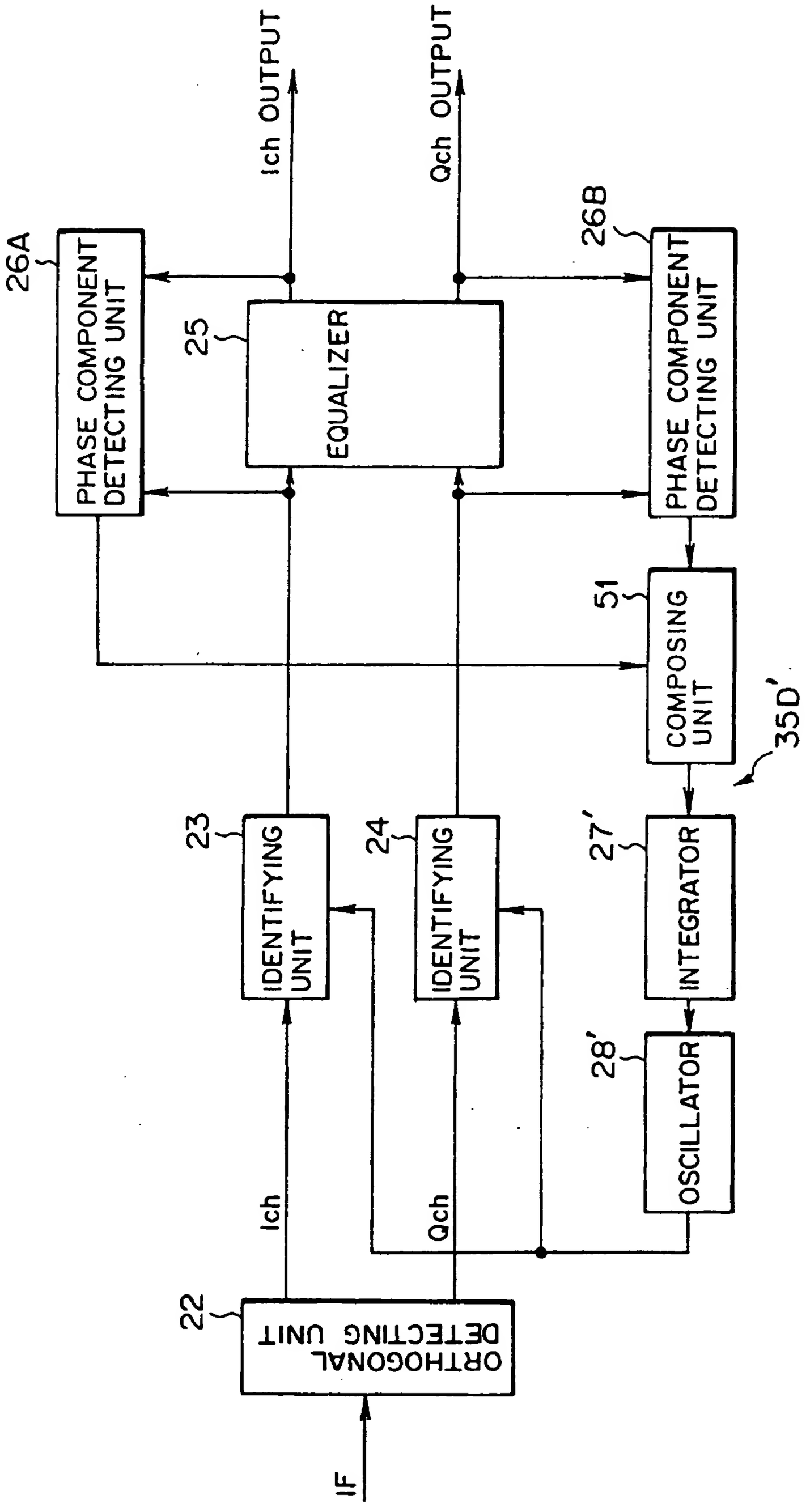

Ich OUTPUT
Qch OUTPUT
26A
PHASE COMPONENT DETECTING UNIT
25
EQUALIZER
26B
PHASE COMPONENT DETECTING UNIT
51
COMPOSING UNIT
35D'
23
IDENTIFYING UNIT
24
IDENTIFYING UNIT
27'
INTEGRATOR
28'
OSCILLATOR
Ich
Qch
22
ORTHOGONAL DETECTING UNIT
IF

FIG. 35

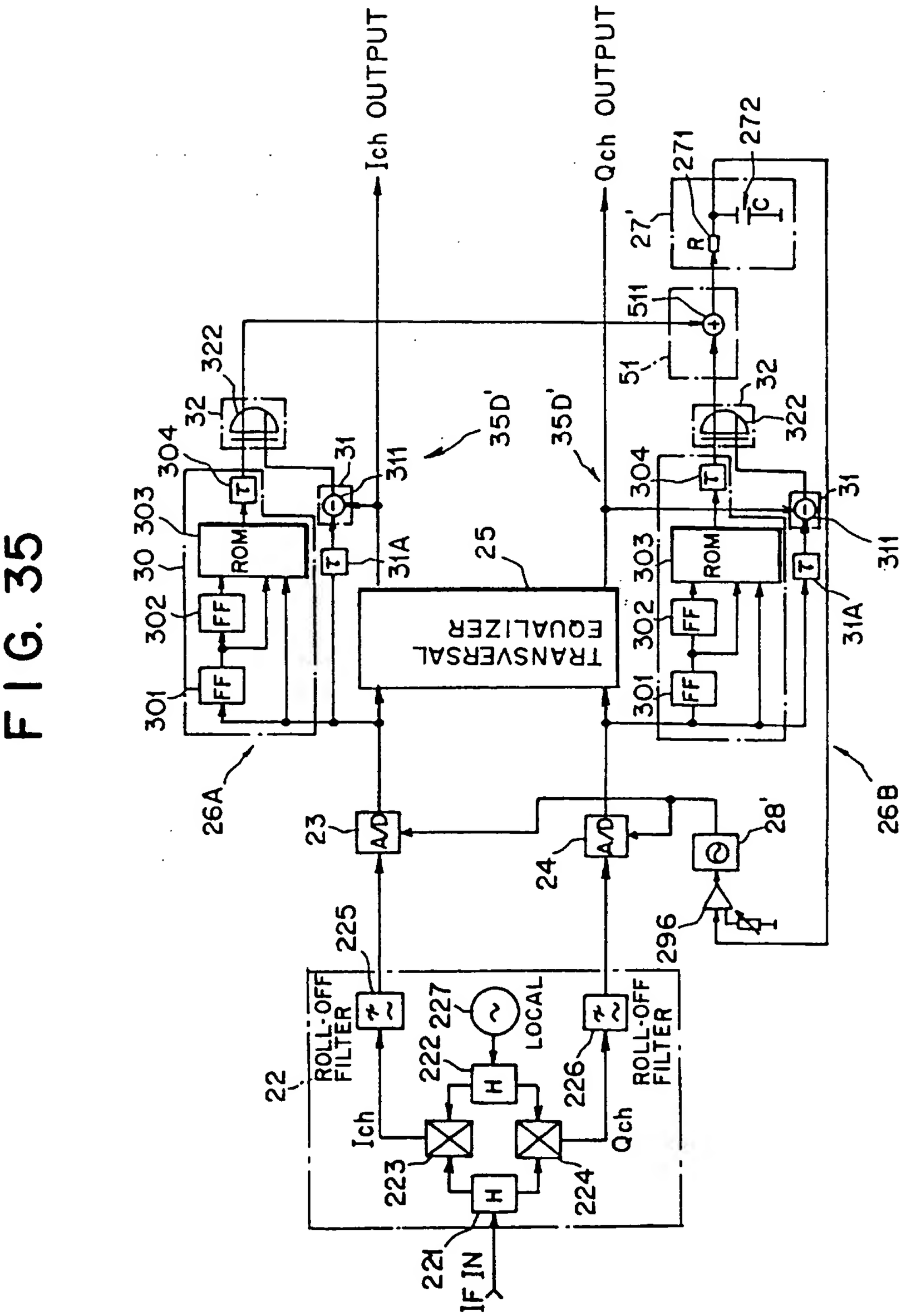

Ich OUTPUT
Qch OUTPUT
271
272
27'
R
Tc
511
51
32
322
304
303
30
302
301
FF
ROM
T
31
311
31A
35D'
25
TRANSVERSAL EQUALIZER
26A
26B
23
24
A/D
28'
225
296
ROLL-OFF FILTER
LOCAL
227
222
226
223
224
22
221
IF IN
Ich
Qch
H

FIG. 36

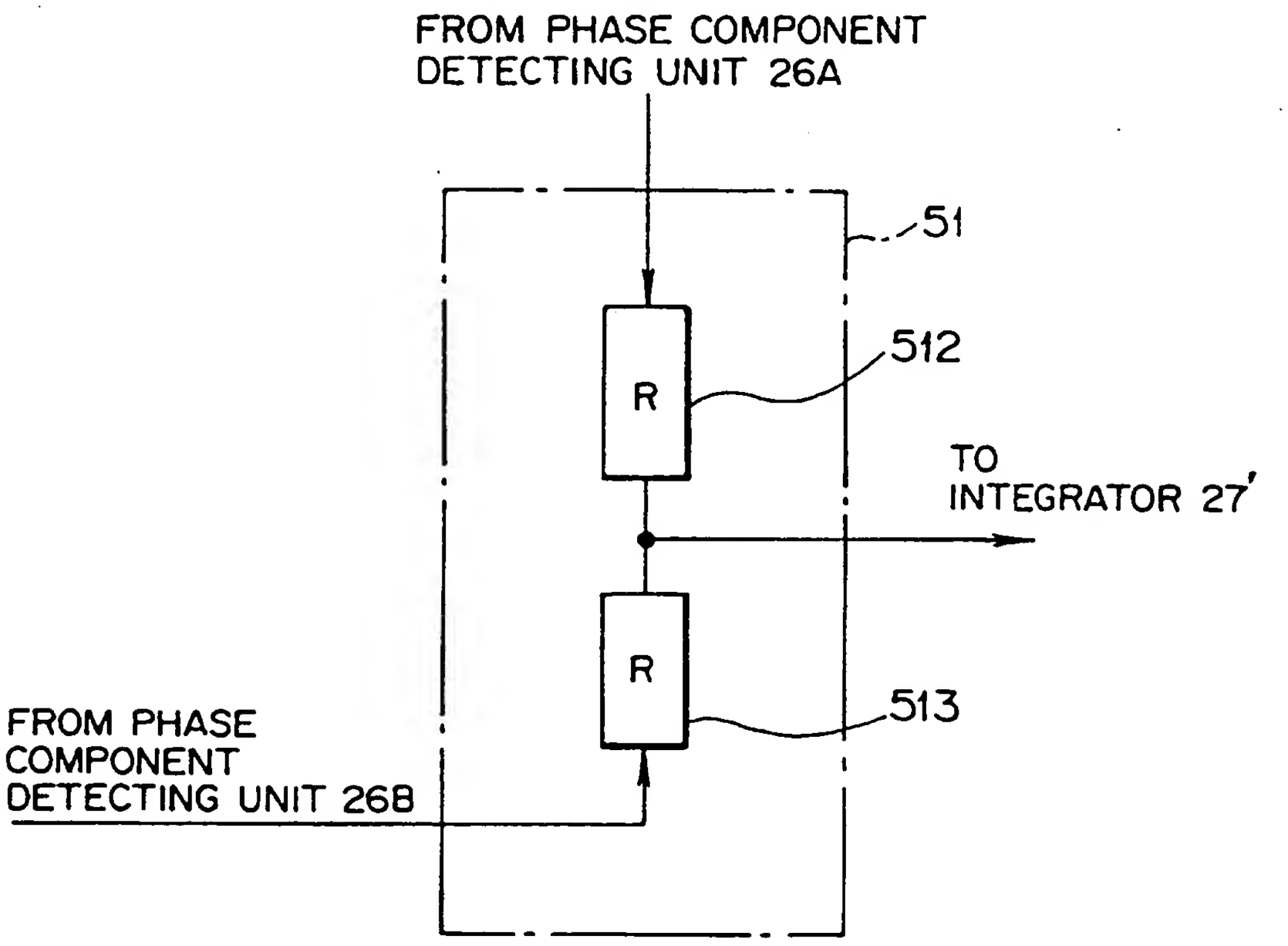

FROM PHASE COMPONENT DETECTING UNIT 26A
51
512
R
TO INTEGRATOR 27'
R
513
FROM PHASE COMPONENT DETECTING UNIT 26B

FIG.37

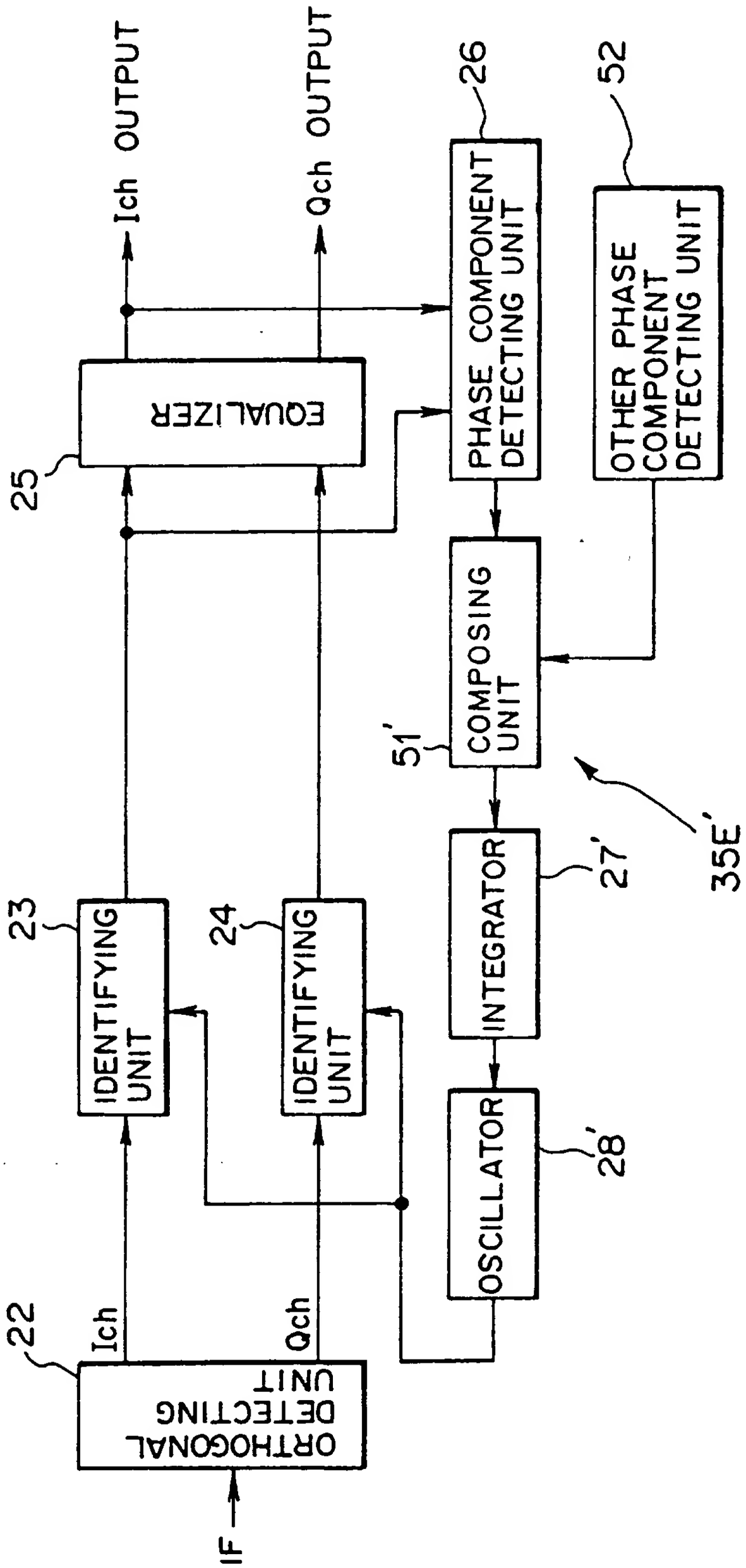

IF
ORTHOGONAL DETECTING UNIT
22
Ich
Qch
IDENTIFYING UNIT
23
IDENTIFYING UNIT
24
EQUALIZER
25
PHASE COMPONENT DETECTING UNIT
26
OTHER PHASE COMPONENT DETECTING UNIT
52
COMPOSING UNIT
51'
INTEGRATOR
27'
OSCILLATOR
28'
35E'
Ich OUTPUT
Qch OUTPUT

FIG. 38

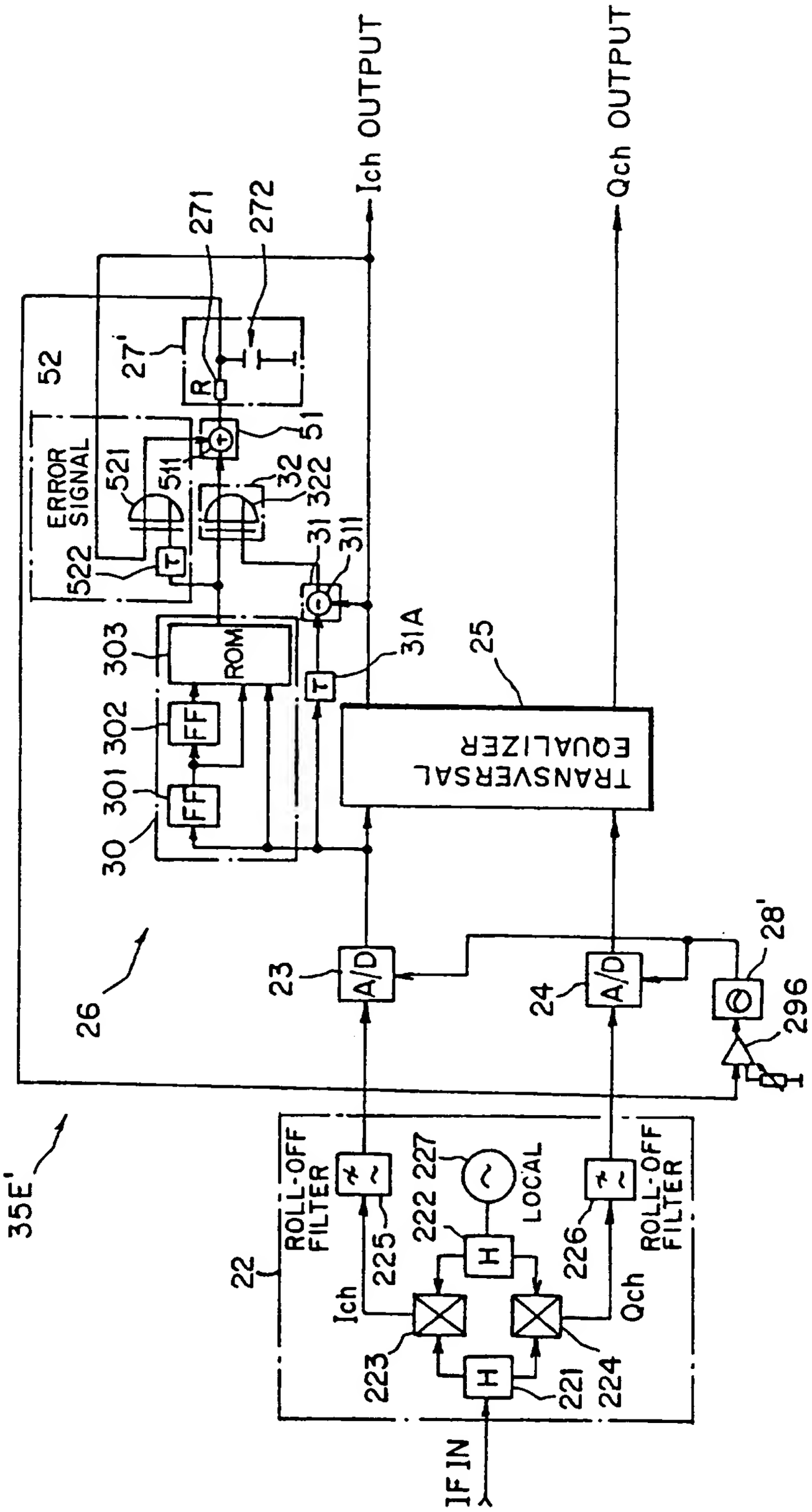

Ich OUTPUT
Qch OUTPUT
271
272
52
27'
R
I
I
51
ERROR SIGNAL
521
511
32
322
522
T
31
311
303
ROM
31A
25
302
FF
TRANSVERSAL EQUALIZER
301
FF
30
26
23
A/D
24
A/D
28'
296
35E'
22
ROLL-OFF FILTER
225
222
227
LOCAL
226
ROLL-OFF FILTER
Ich
Qch
H
223
221
224
IF IN

FIG.39

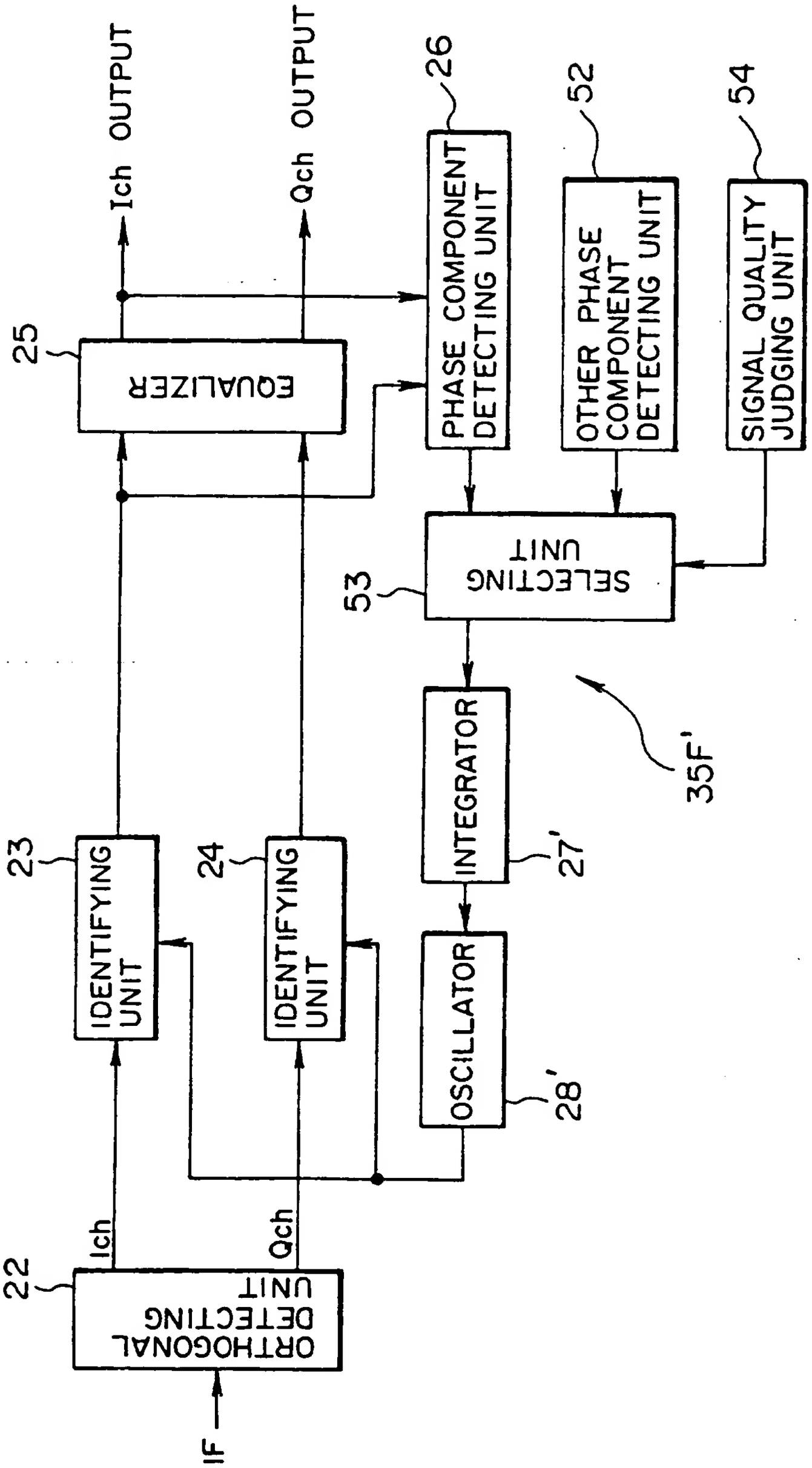

IF
ORTHOGONAL DETECTING UNIT
22
Ich
Qch
IDENTIFYING UNIT
23
IDENTIFYING UNIT
24
EQUALIZER
25
Ich OUTPUT
Qch OUTPUT
PHASE COMPONENT DETECTING UNIT
26
OTHER PHASE COMPONENT DETECTING UNIT
52
SIGNAL QUALITY JUDGING UNIT
54
SELECTING UNIT
53
INTEGRATOR
27'
OSCILLATOR
28'
35F'

FIG. 40

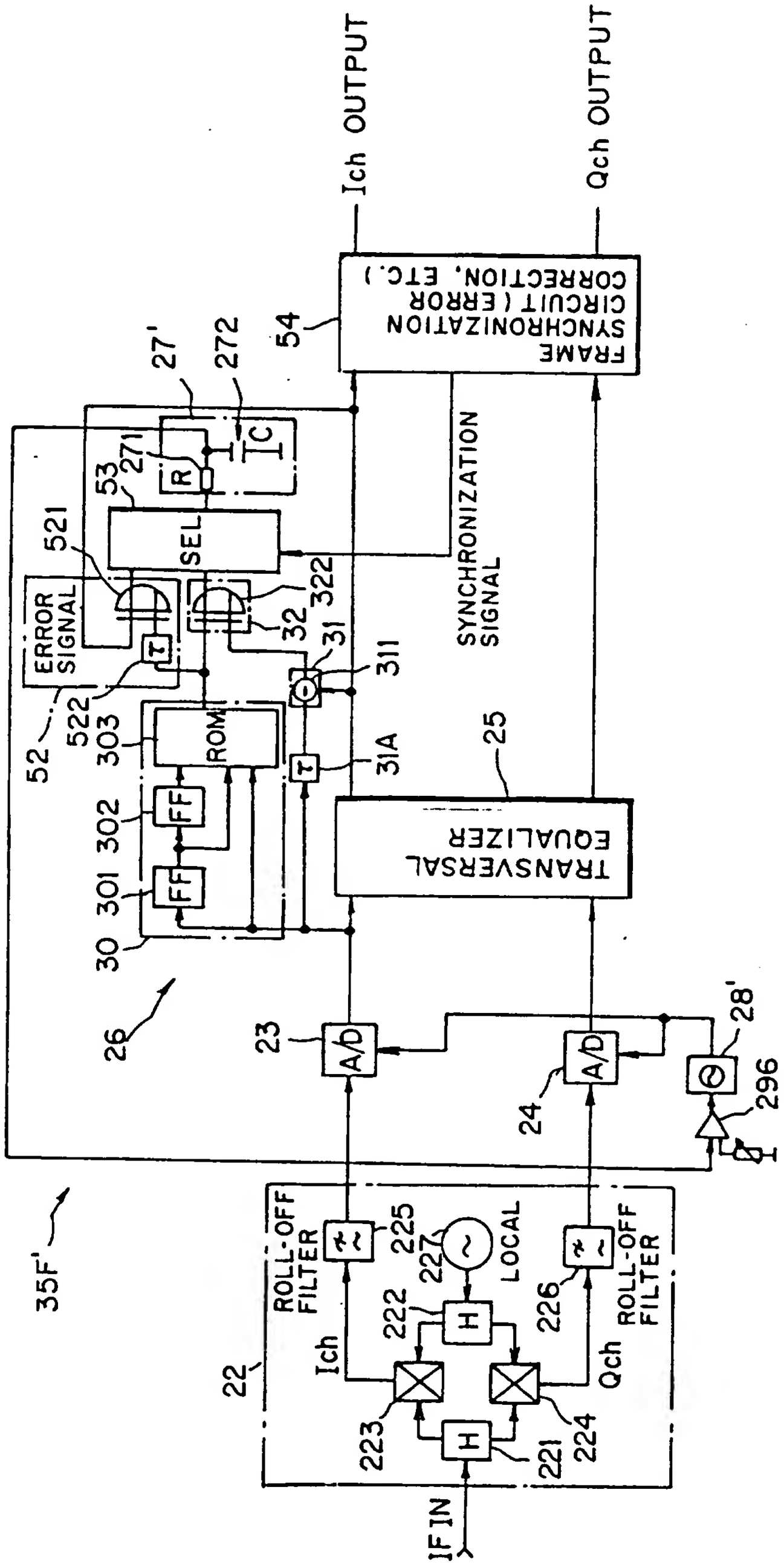

Ich OUTPUT
Qch OUTPUT
FRAME SYNCHRONIZATION CIRCUIT (ERROR CORRECTION, ETC.)
54
27'
272
271
53
R
IC
I
SEL
521
ERROR SIGNAL
522
52
T
32
322
31
311
SYNCHRONIZATION SIGNAL
303
ROM
31A
25
302
FF
301
30
TRANSVERSAL EQUALIZER
26
23
A/D
24
28'
296
35F'
ROLL-OFF FILTER
225
227
LOCAL
222
H
226
Ich
Qch
22
223
221
224
IF IN

FIG. 41

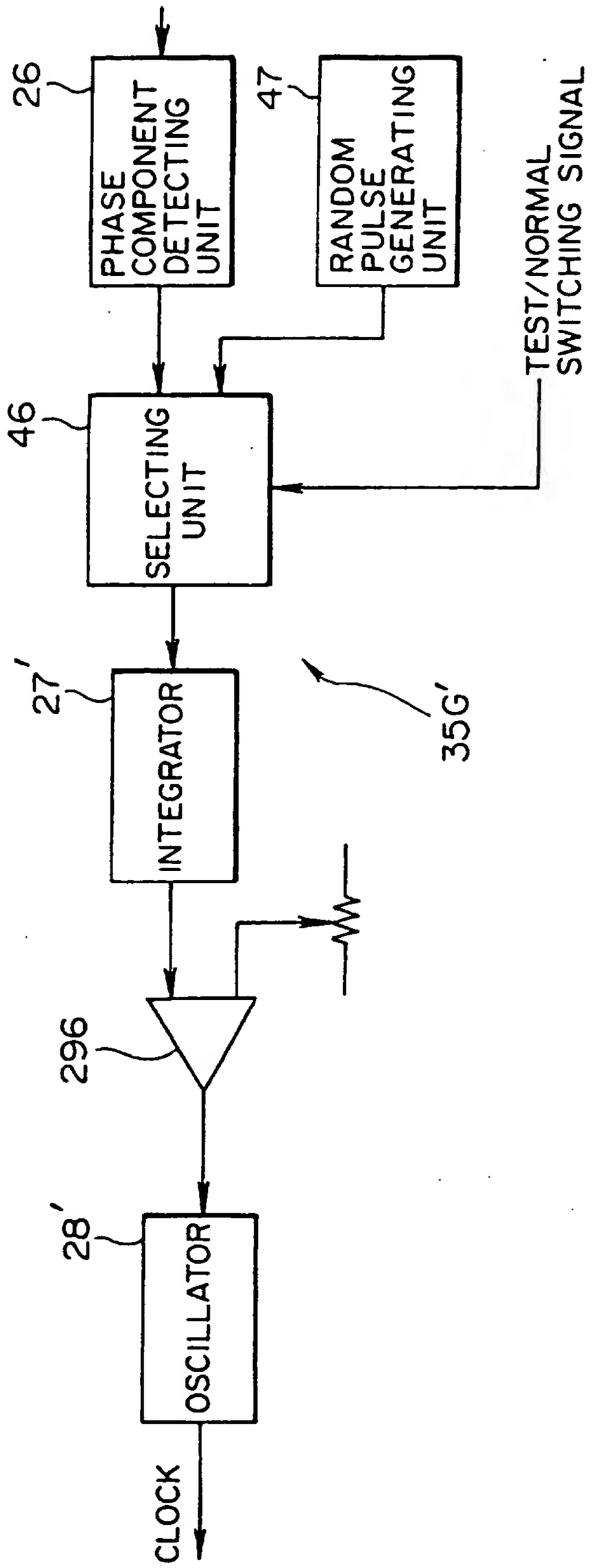

26
PHASE COMPONENT DETECTING UNIT
47
RANDOM PULSE GENERATING UNIT
TEST/NORMAL SWITCHING SIGNAL
46
SELECTING UNIT
27'
INTEGRATOR
35G'
296
28'
OSCILLATOR
CLOCK

FIG. 42

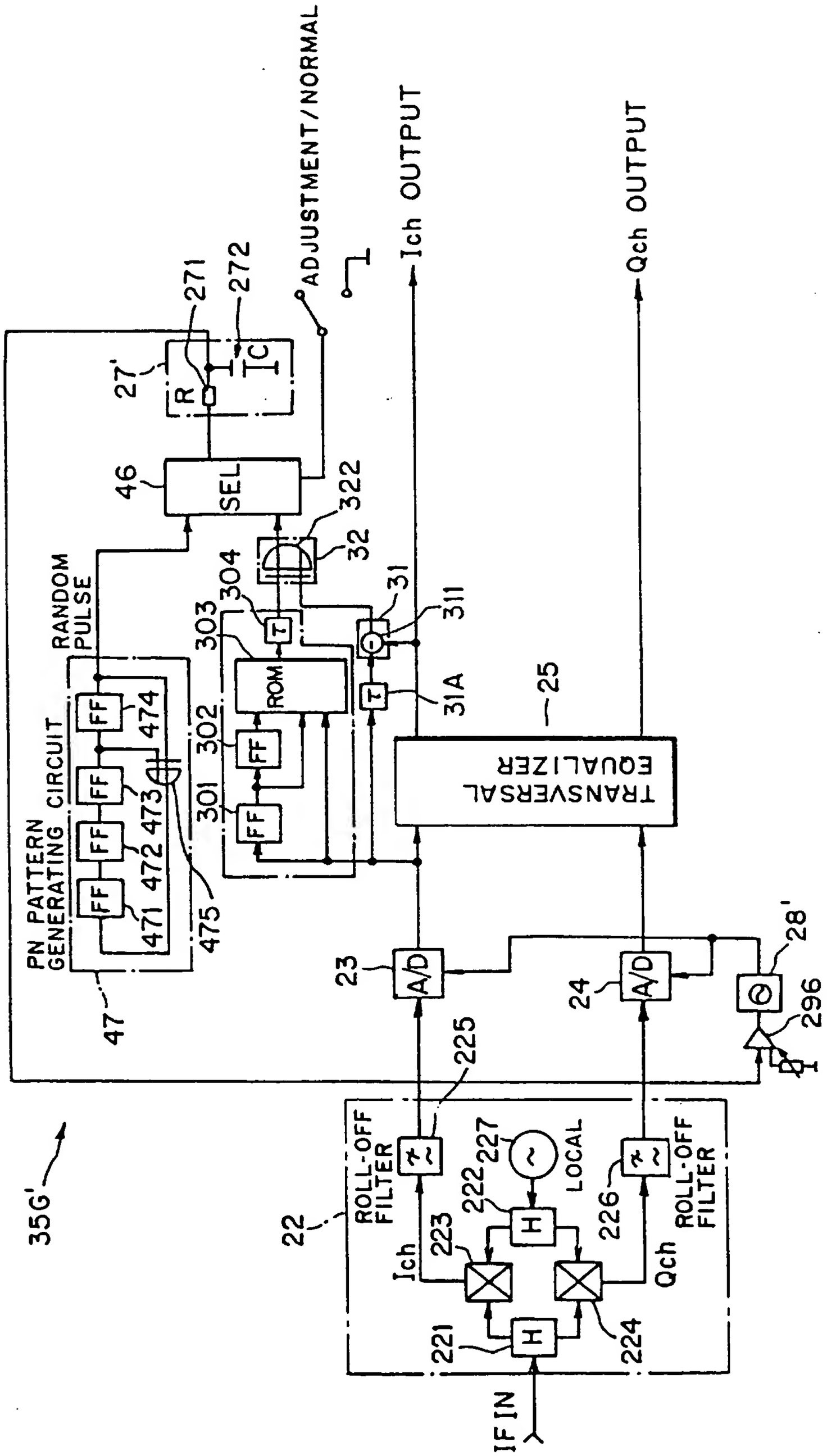

35G'
PN PATTERN GENERATING CIRCUIT
RANDOM PULSE
FF
471
472
473
474
475
271
272
ADJUSTMENT/NORMAL
Ich OUTPUT
Qch OUTPUT
27'
R
I
IC
46
SEL
322
32
304
303
302
301
ROM
T
31
311
31A
25
TRANSVERSAL EQUALIZER
23
24
A/D
28'
296
47'
225
ROLL-OFF FILTER
22
227
LOCAL
222
223
226
221
224
H
Ich
Qch
IF IN

FIG.43

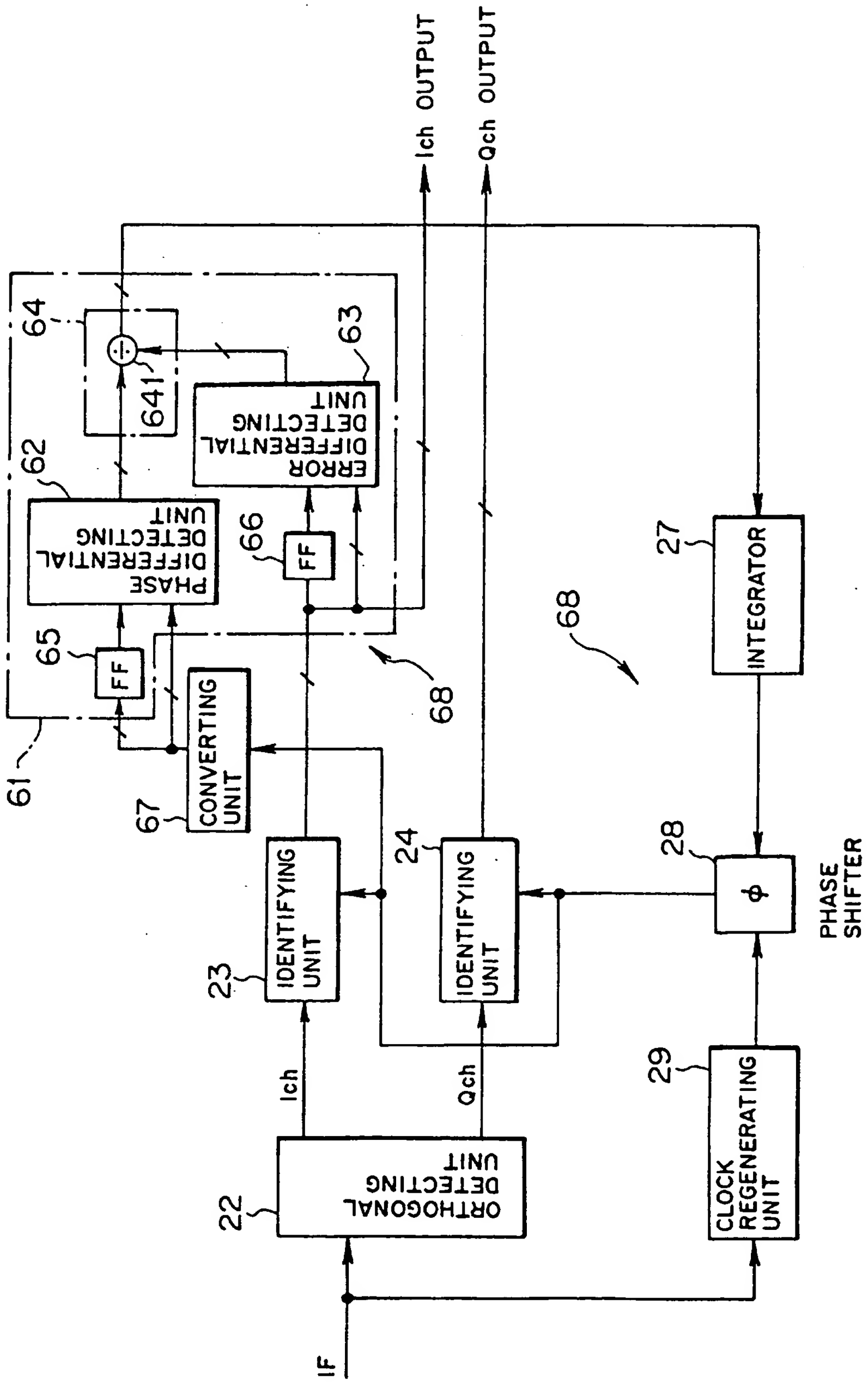

Ich OUTPUT
Qch OUTPUT
64
641
63
ERROR DIFFERENTIAL DETECTING UNIT
62
PHASE DIFFERENTIAL DETECTING UNIT
66
FF
65
FF
61
68
67
CONVERTING UNIT
24
IDENTIFYING UNIT
23
IDENTIFYING UNIT
Ich
Qch
22
ORTHOGONAL DETECTING UNIT
IF
68
27
INTEGRATOR
28
Φ
PHASE SHIFTER
29
CLOCK REGENERATING UNIT

FIG. 44

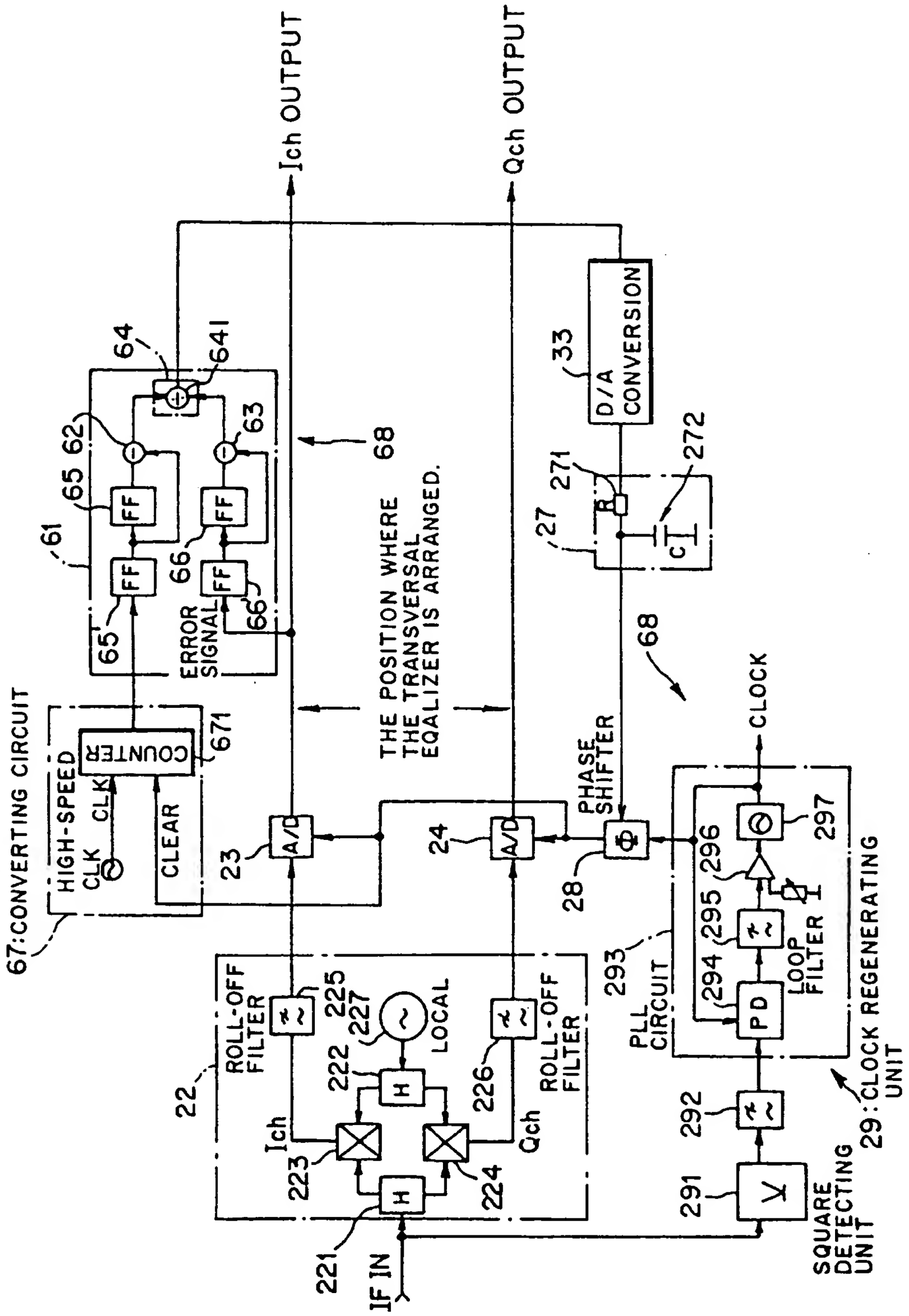

Ich OUTPUT
Qch OUTPUT
64
641
62
63
65
66
61
FF
65'
66'
ERROR SIGNAL
68
THE POSITION WHERE THE TRANSVERSAL EQALIZER IS ARRANGED.
D/A CONVERSION
33
271
272
27
CI
68
PHASE SHIFTER
CLOCK
HIGH-SPEED AGC CONVERTING CIRCUIT
CLK
COUNTER
671
CLEAR
23
24
A/D
28
296
297
295
294
PD
LOOP FILTER
293
PLL CIRCUIT
292
291
SQUARE DETECTING UNIT
29:CLOCK REGENERATING UNIT
67:
22
ROLL-OFF FILTER
225
227
LOCAL
222
226
Ich
Qch
223
224
H
221
IF IN

FIG. 45

FIG.46

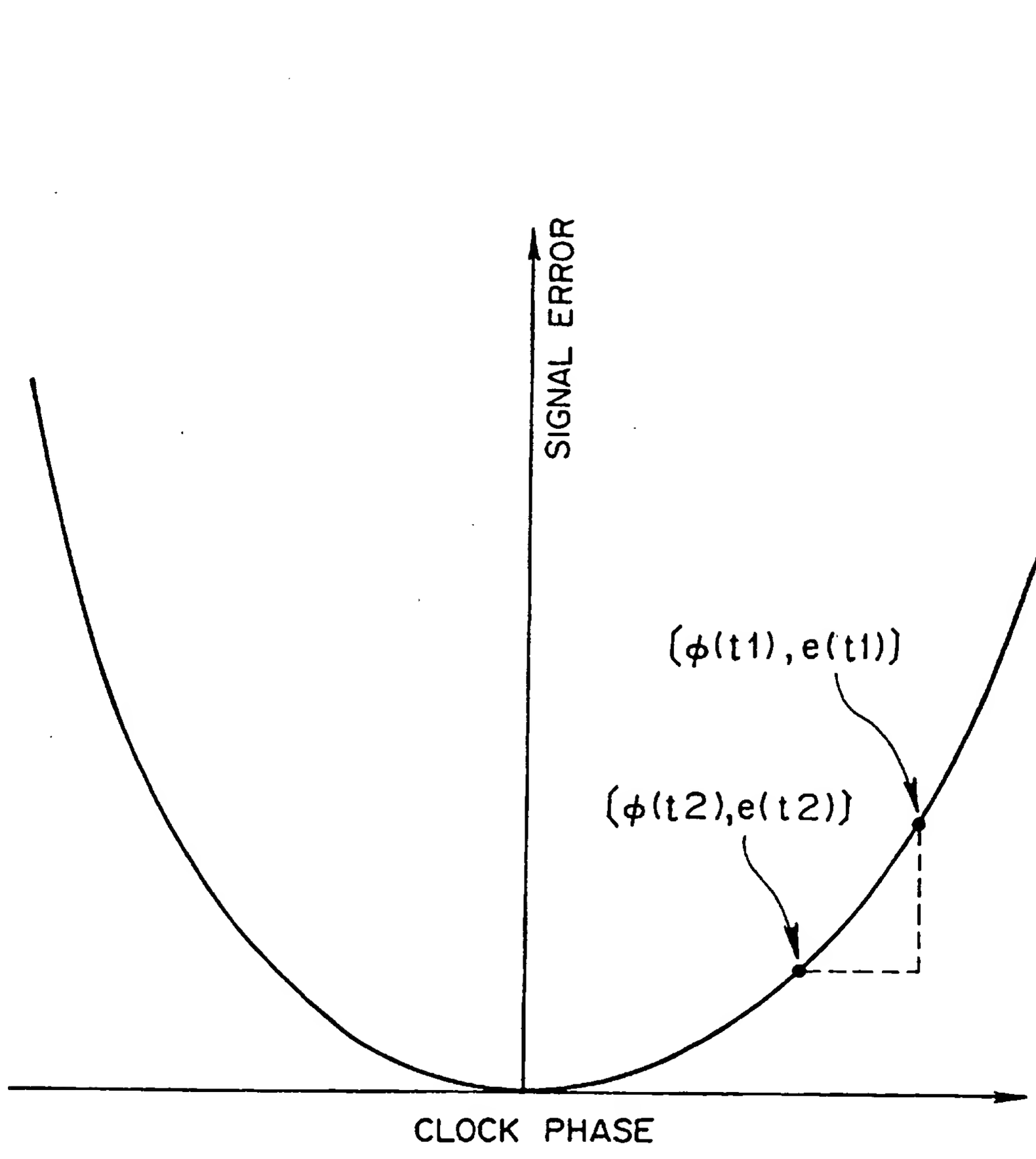


FIG. 47

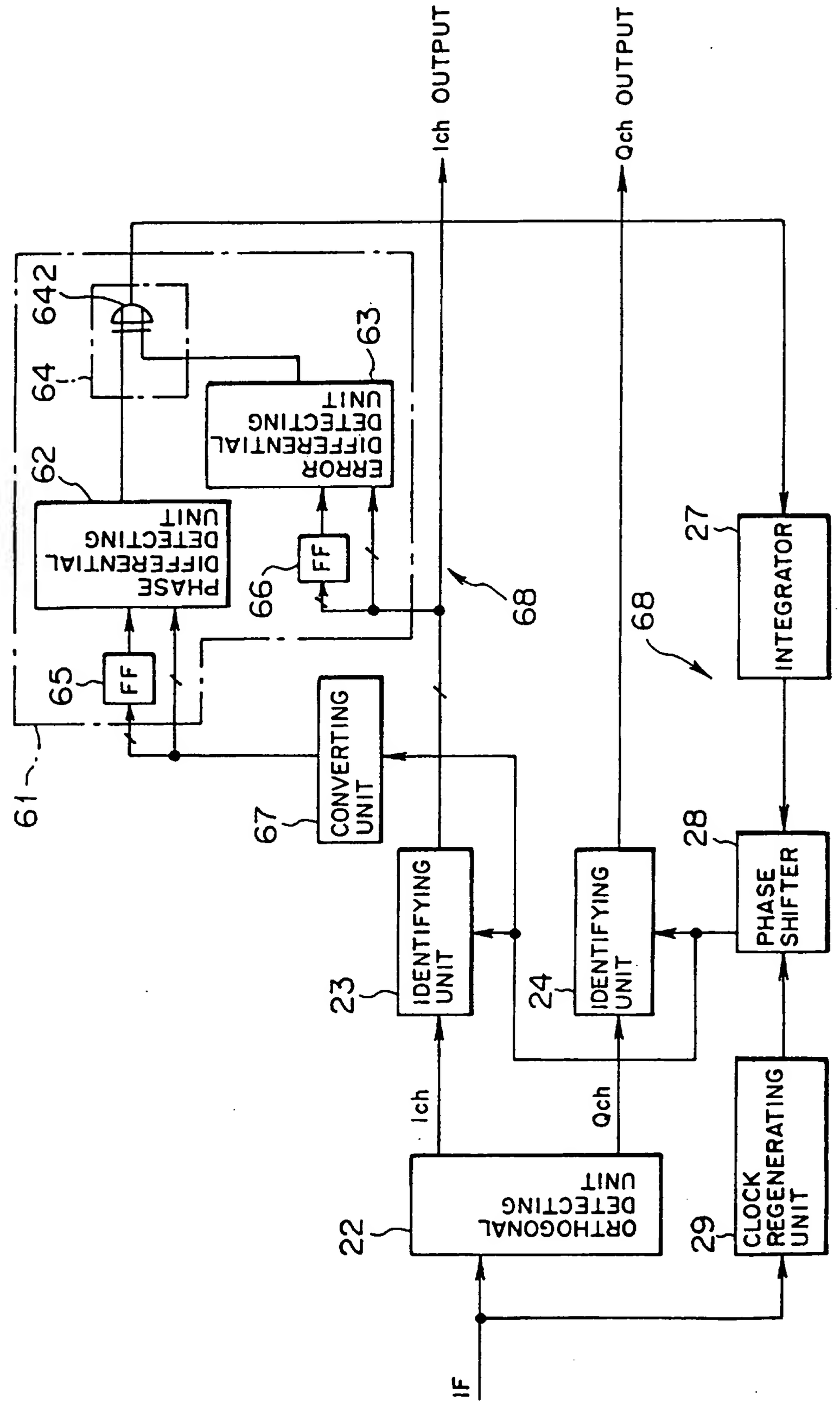

Ich OUTPUT
Qch OUTPUT
61
62
PHASE DIFFERENTIAL DETECTING UNIT
63
ERROR DIFFERENTIAL DETECTING UNIT
64
642
65
FF
66
FF
67
CONVERTING UNIT
68
IDENTIFYING UNIT
23
IDENTIFYING UNIT
24
ORTHOGONAL DETECTING UNIT
22
Ich
Qch
IF
68
27
INTEGRATOR
28
PHASE SHIFTER
29
CLOCK REGENERATING UNIT

FIG. 48

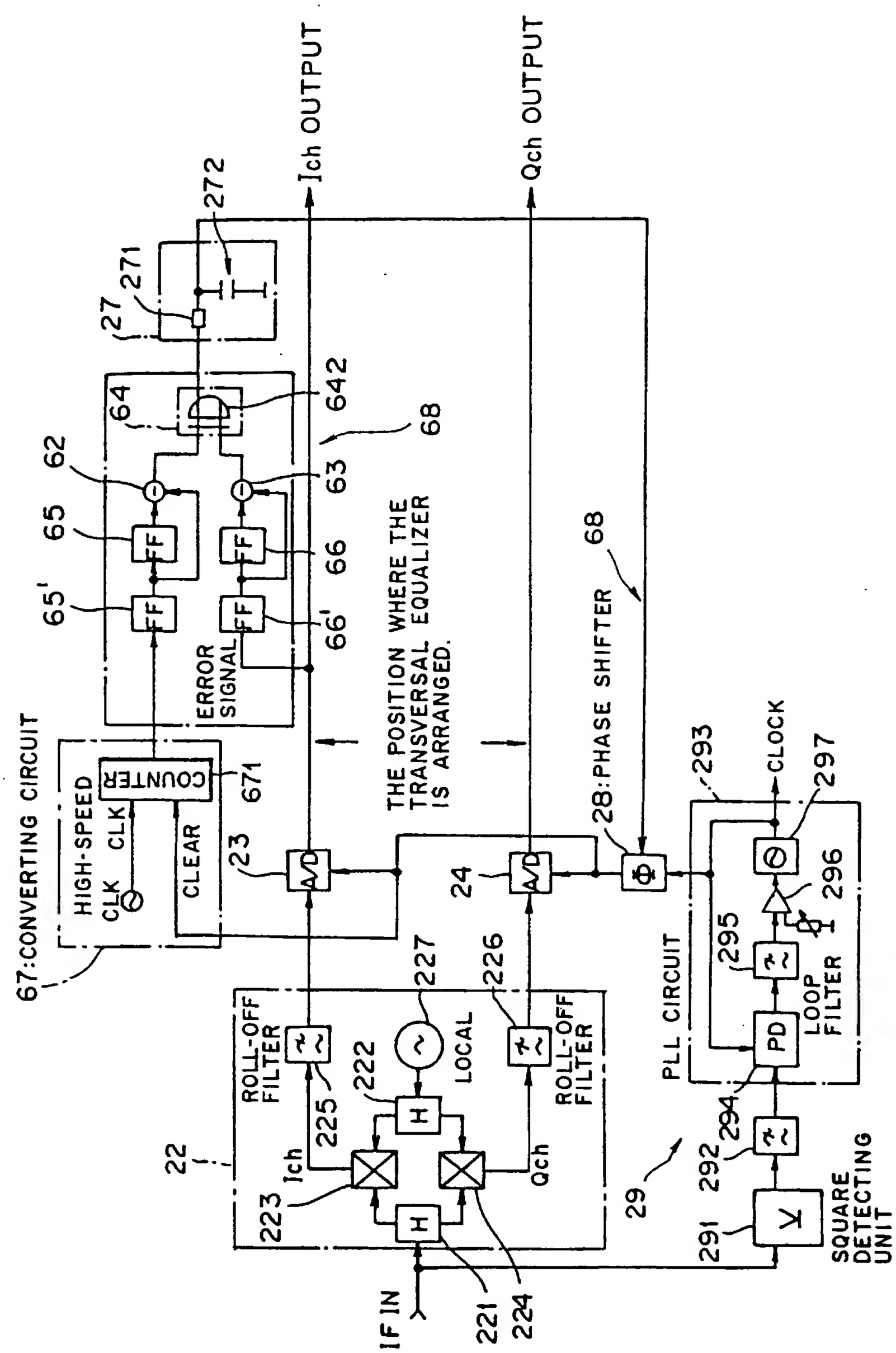

Ich OUTPUT
Qch OUTPUT
272
271
27
64
642
62
63
65
66
65'
66'
68
FF
ERROR SIGNAL
THE POSITION WHERE THE TRANSVERSAL EQUALIZER IS ARRANGED.
67:CONVERTING CIRCUIT
HIGH-SPEED CLK
CLK
COUNTER
671
CLEAR
23
24
A/D
227
226
28:PHASE SHIFTER
293
CLOCK
297
296
295
PLL CIRCUIT
PD
LOOP FILTER
294
292
291
SQUARE DETECTING UNIT
29
22
ROLL-OFF FILTER
225
222
LOCAL
223
Ich
Qch
IF IN
221
224

FIG.49

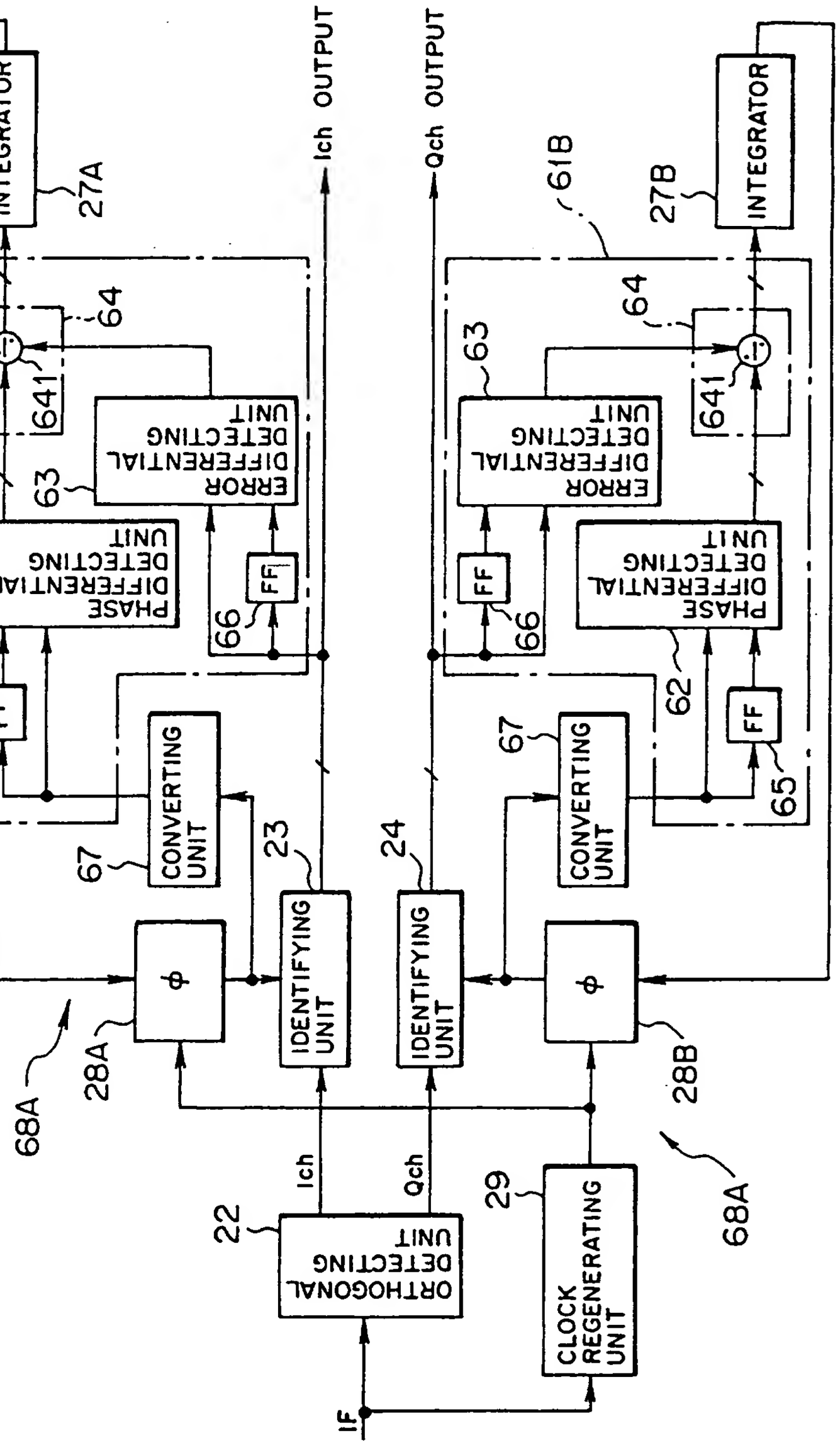

INTEGRATOR
27A
Ich OUTPUT
Qch OUTPUT
61B
27B
INTEGRATOR
64
641
63
ERROR DIFFERENTIAL DETECTING UNIT
62
PHASE DIFFERENTIAL DETECTING UNIT
FF
66
65
67
CONVERTING UNIT
61A
23
24
IDENTIFYING UNIT
φ
28A
28B
68A
Ich
Qch
22
ORTHOGONAL DETECTING UNIT
29
CLOCK REGENERATING UNIT
IF

FIG. 50

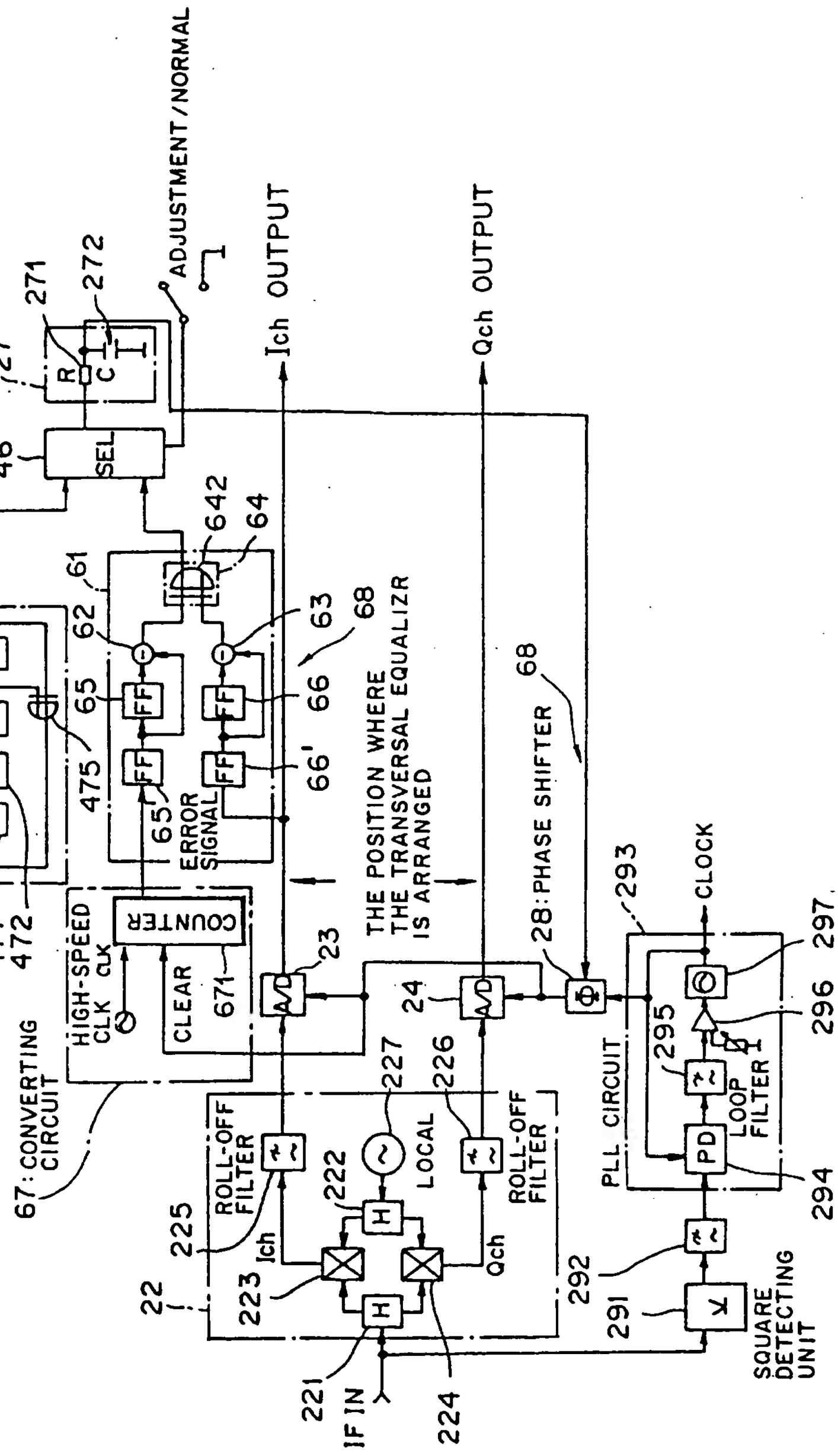

ADJUSTMENT/NORMAL
271
272
27
R
C
I
Ich OUTPUT
Qch OUTPUT
46
SEL
RANDOM PULSE
474
473
PN PATTERN GENERATING CIRCUIT
47
471
472
642
64
61
62
63
68
65
66
66'
65'
ERROR SIGNAL
475
THE POSITION WHERE THE TRANSVERSAL EQUALIZR IS ARRANGED
68
28: PHASE SHIFTER
HIGH-SPEED CLK CLK
COUNTER
CLEAR
671
23
24
293
CLOCK
67: CONVERTING CIRCUIT
227
226
ROLL-OFF FILTER
225
222
LOCAL
ROLL-OFF FILTER
PLL CIRCUIT
296
297
PD
LOOP FILTER
294
Ich
Qch
223
22
292
291
SQUARE DETECTING UNIT
221
IF IN
224

FIG.51

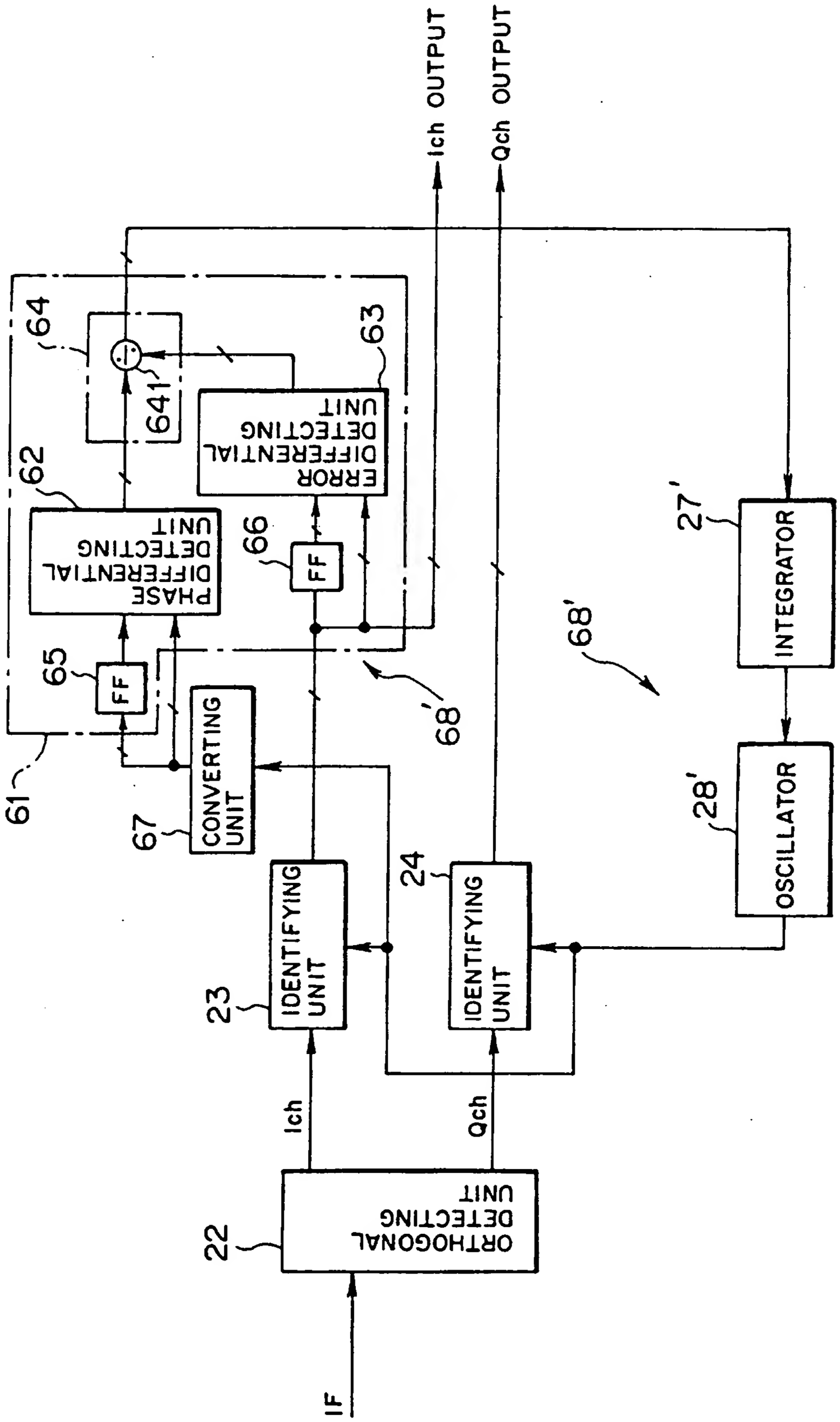

IF
ORTHOGONAL DETECTING UNIT
22
Ich
Qch
IDENTIFYING UNIT
23
IDENTIFYING UNIT
24
CONVERTING UNIT
67
FF
65
FF
66
PHASE DIFFERENTIAL DETECTING UNIT
62
ERROR DIFFERENTIAL DETECTING UNIT
63
64
641
61
68'
68'
INTEGRATOR
27'
OSCILLATOR
28'
Ich OUTPUT
Qch OUTPUT

FIG. 52

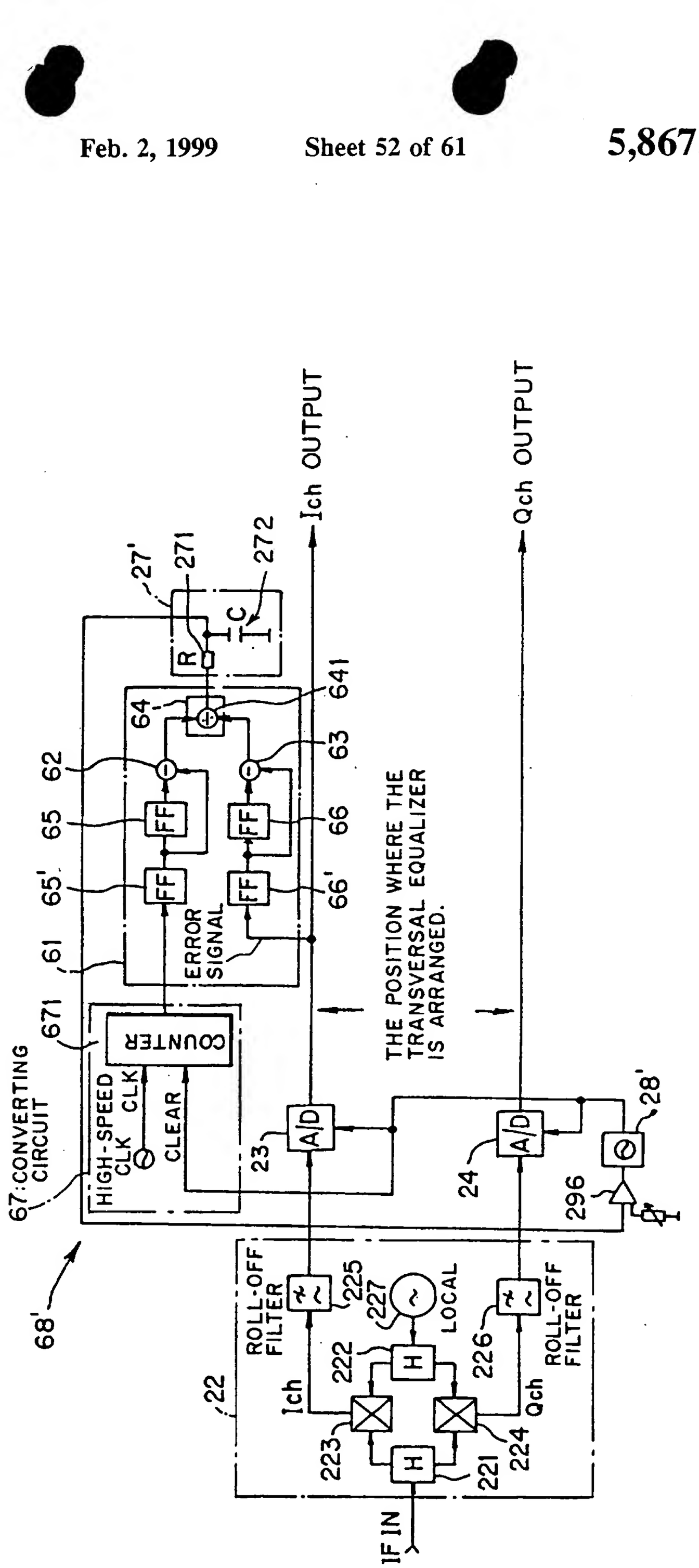

67:CONVERTING CIRCUIT
HIGH-SPEED CLK
CLK
CLEAR
COUNTER
671
61
65'
65
62
64
641
63
66
66'
FF
ERROR SIGNAL
THE POSITION WHERE THE TRANSVERSAL EQUALIZER IS ARRANGED.
Ich OUTPUT
Qch OUTPUT
27'
271
272
R
C
I
23
24
A/D
28'
296
68'
22
ROLL-OFF FILTER
225
227
LOCAL
222
226
Ich
Qch
223
224
221
H
IF IN

FIG. 53

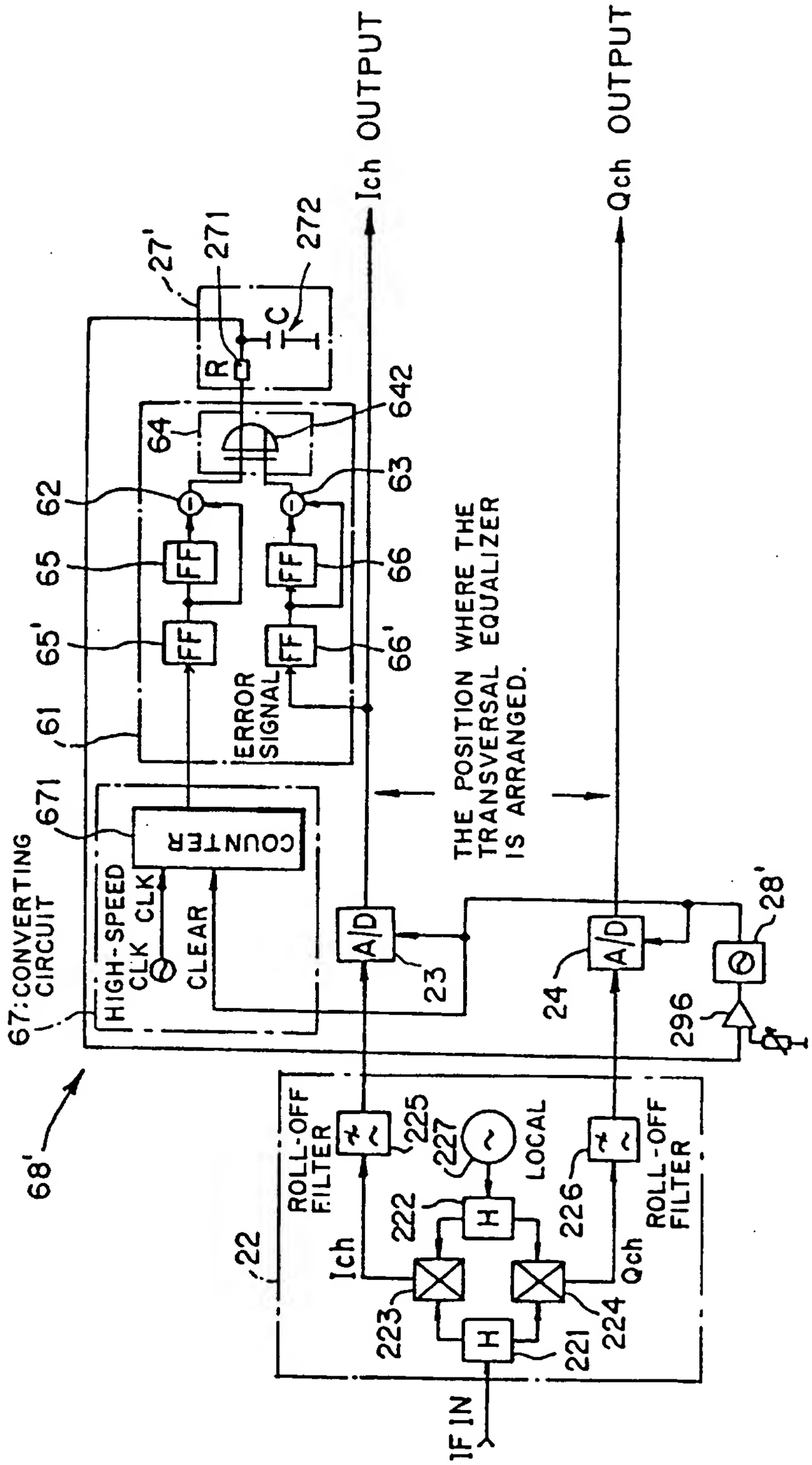

Ich OUTPUT
Qch OUTPUT
271
272
27'
R
C
64
642
62
63
65
66
65'
66'
61
ERROR SIGNAL
671
COUNTER
67:CONVERTING CIRCUIT
HIGH-SPEED CLK
CLK
CLEAR
THE POSITION WHERE THE TRANSVERSAL EQUALIZER IS ARRANGED.
A/D
23
24
28'
296
68'
ROLL-OFF FILTER
225
227
LOCAL
222
226
Ich
Qch
223
224
221
H
IF IN

FIG. 54

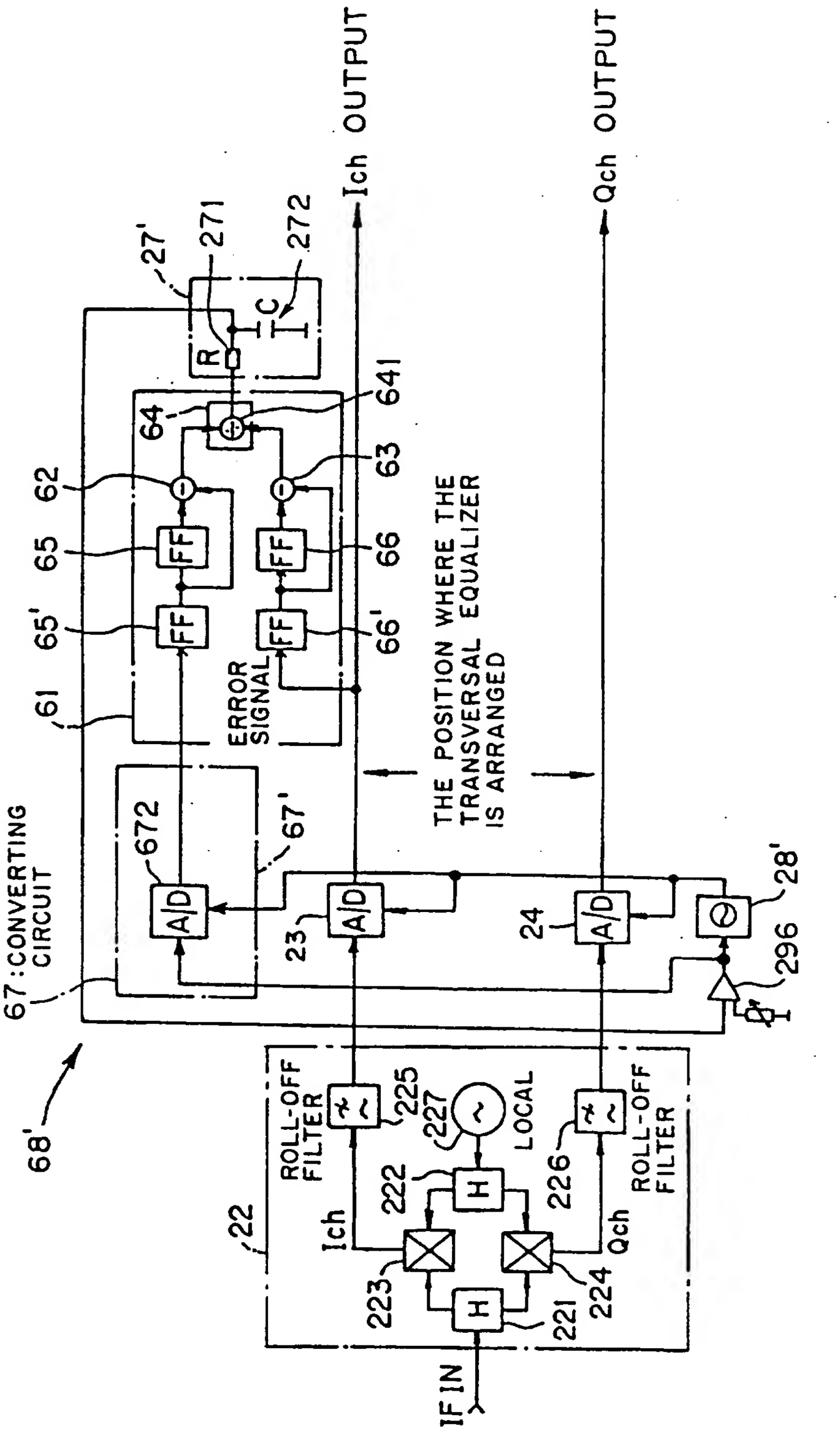

67:CONVERTING CIRCUIT
68'
ROLL-OFF FILTER
ROLL-OFF FILTER
LOCAL
IF IN
Ich
Qch
Ich OUTPUT
Qch OUTPUT
ERROR SIGNAL
THE POSITION WHERE THE TRANSVERSAL EQUALIZER IS ARRANGED
A/D
FF
H
R
C
61
62
63
64
65
65'
66
66'
67'
672
641
271
272
27'
22
23
24
221
222
223
224
225
226
227
28'
296

FIG.55

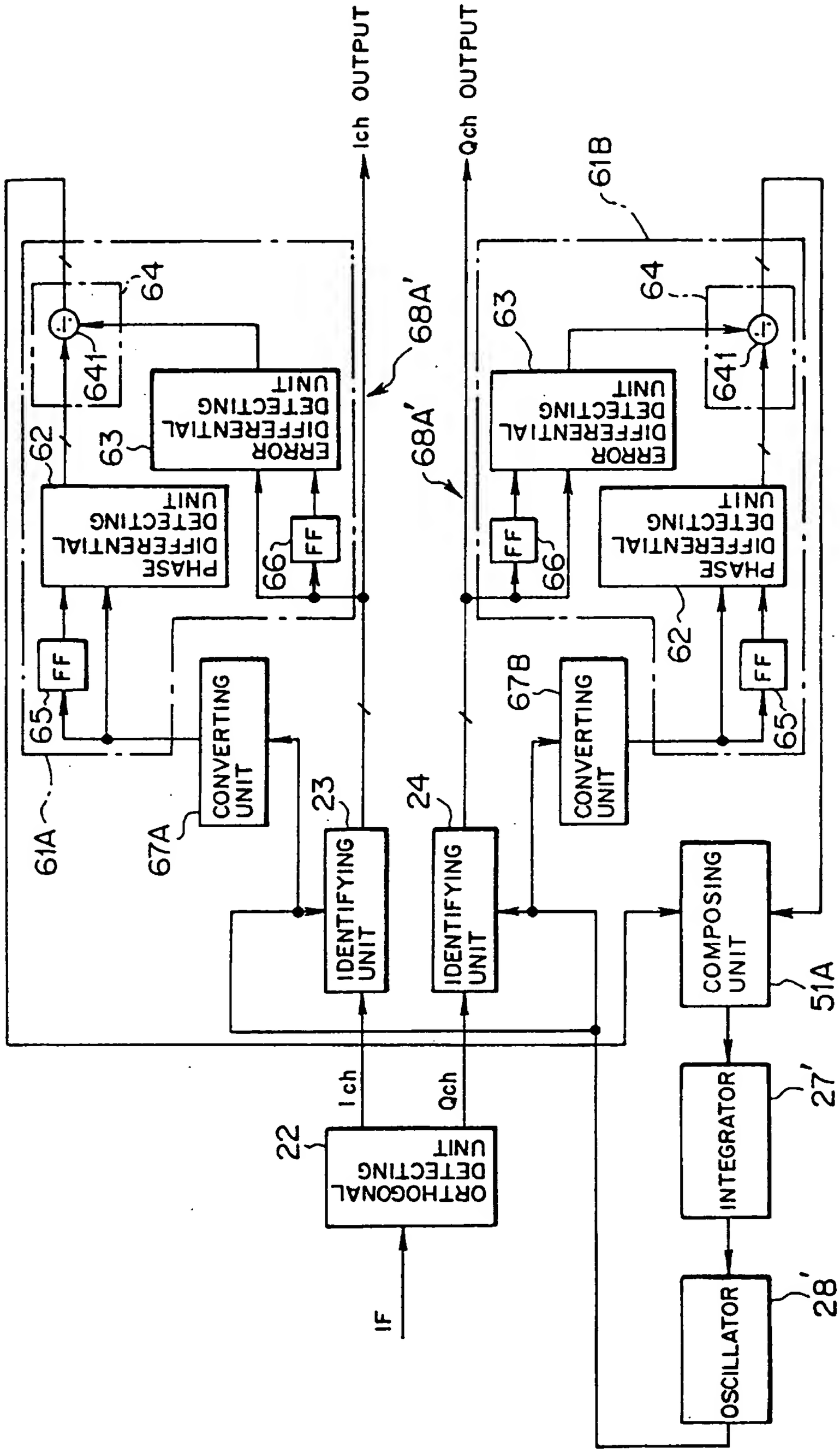

Ich OUTPUT
Qch OUTPUT
61B
64
641
63
68A
68A'
ERROR DIFFERENTIAL DETECTING UNIT
62
PHASE DIFFERENTIAL DETECTING UNIT
66
FF
65
61A
67A
CONVERTING UNIT
67B
23
24
IDENTIFYING UNIT
COMPOSING UNIT
51A
I ch
Qch
22
ORTHOGONAL DETECTING UNIT
IF
INTEGRATOR
27'
OSCILLATOR
28'

FIG. 56

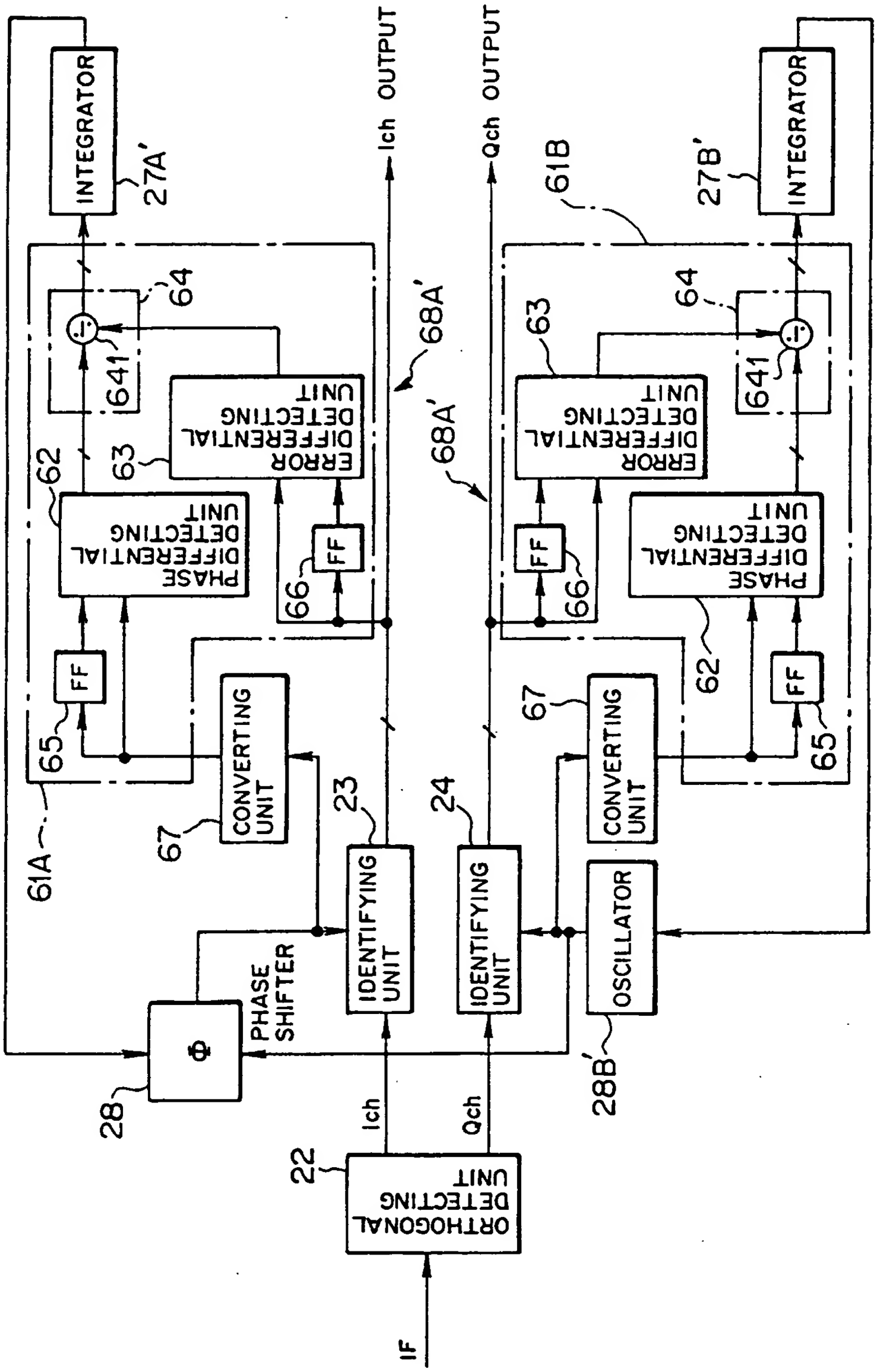

INTEGRATOR
27A'
Ich OUTPUT
Qch OUTPUT
61B
27B'
INTEGRATOR
64
641
63
ERROR DIFFERENTIAL DETECTING UNIT
68A'
68A'
62
PHASE DIFFERENTIAL DETECTING UNIT
FF
66
FF
65
61A
67
CONVERTING UNIT
23
24
IDENTIFYING UNIT
OSCILLATOR
28B'
PHASE SHIFTER
Φ
28
Ich
Qch
22
ORTHOGONAL DETECTING UNIT
IF

FIG.57

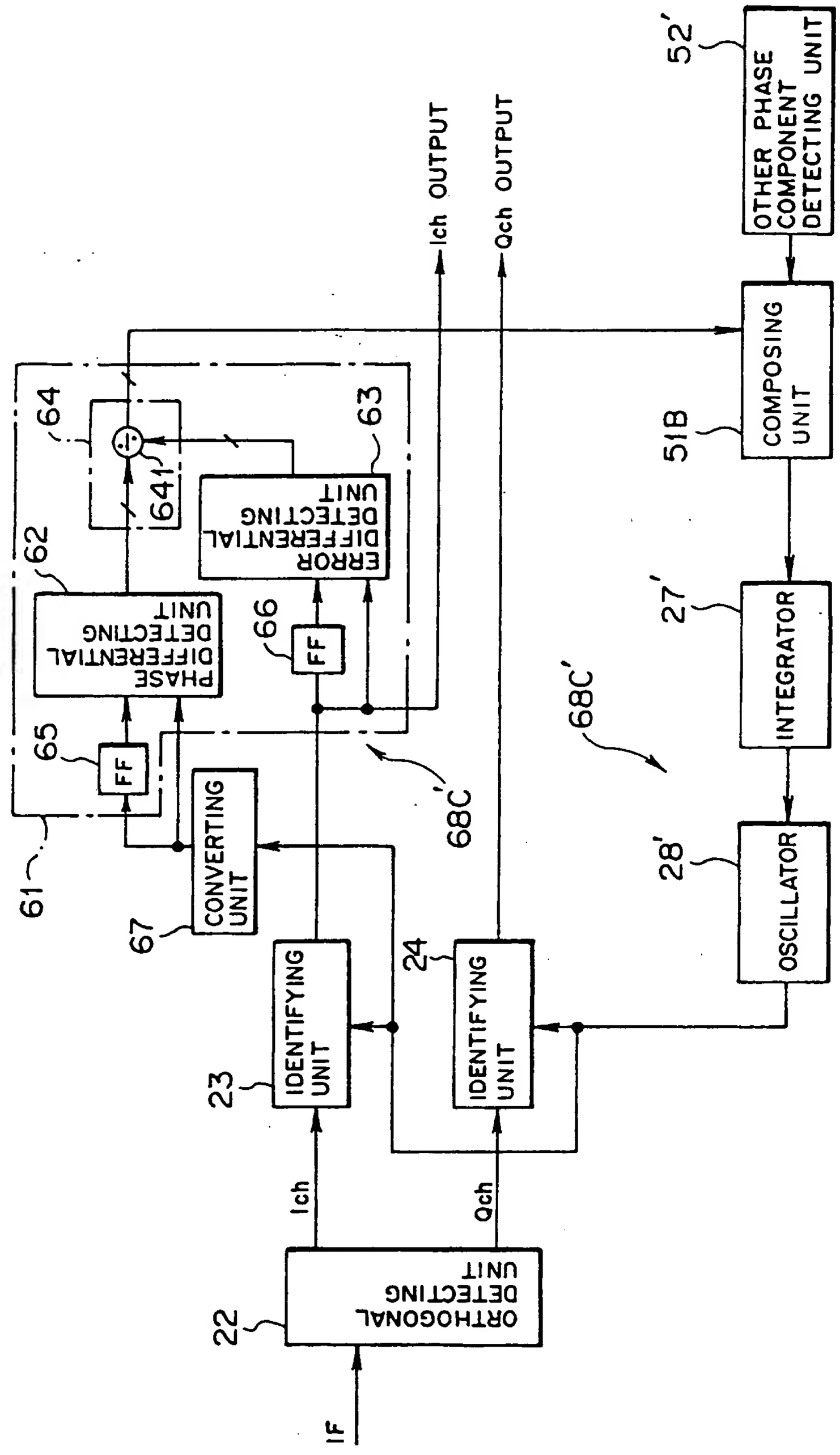

IF
ORTHOGONAL DETECTING UNIT
22
Ich
Qch
IDENTIFYING UNIT
23
IDENTIFYING UNIT
24
Ich OUTPUT
Qch OUTPUT
OTHER PHASE COMPONENT DETECTING UNIT
52'
COMPOSING UNIT
51B
INTEGRATOR
27'
OSCILLATOR
28'
68C'
68C'
61
CONVERTING UNIT
67
FF
65
FF
66
PHASE DIFFERENTIAL DETECTING UNIT
62
ERROR DIFFERENTIAL DETECTING UNIT
63
64
641

FIG.58

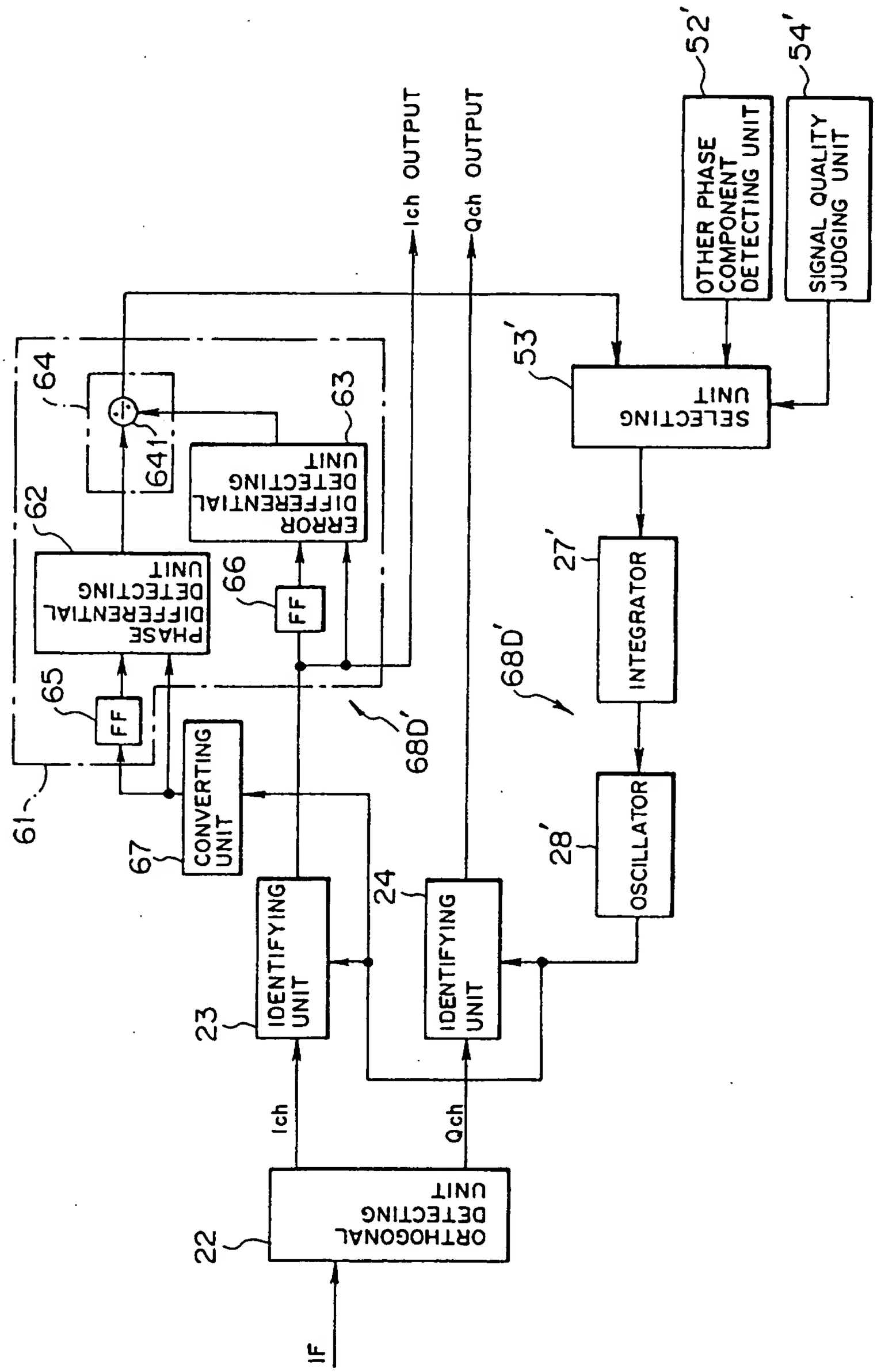

IF
ORTHOGONAL DETECTING UNIT
22
Ich
Qch
IDENTIFYING UNIT
23
IDENTIFYING UNIT
24
CONVERTING UNIT
67
PHASE DIFFERENTIAL DETECTING UNIT
62
ERROR DIFFERENTIAL DETECTING UNIT
63
64
641
65
FF
66
FF
61
68D'
68D'
SELECTING UNIT
53'
INTEGRATOR
27'
OSCILLATOR
28'
OTHER PHASE COMPONENT DETECTING UNIT
52'
SIGNAL QUALITY JUDGING UNIT
54'

FIG. 59

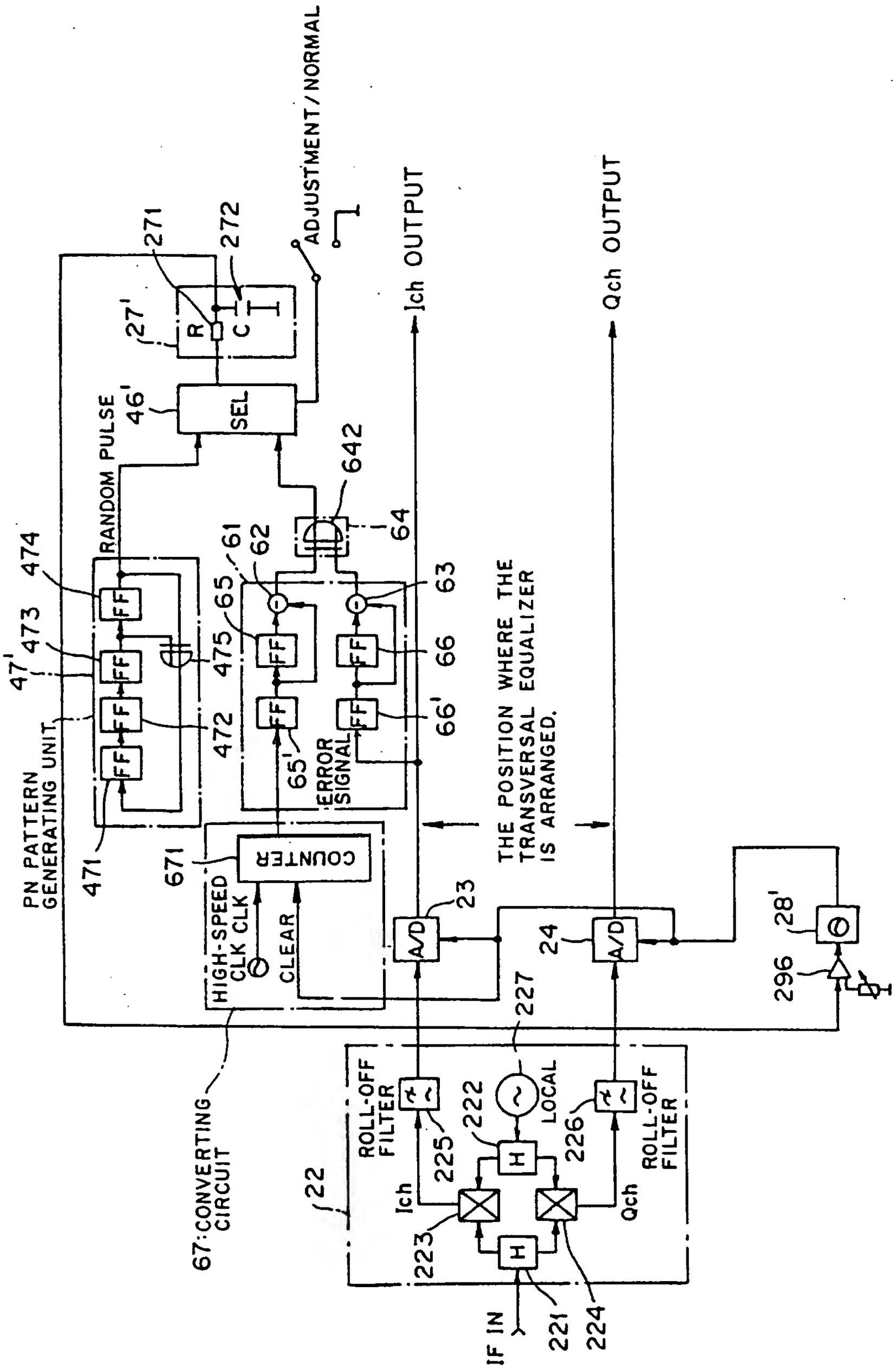
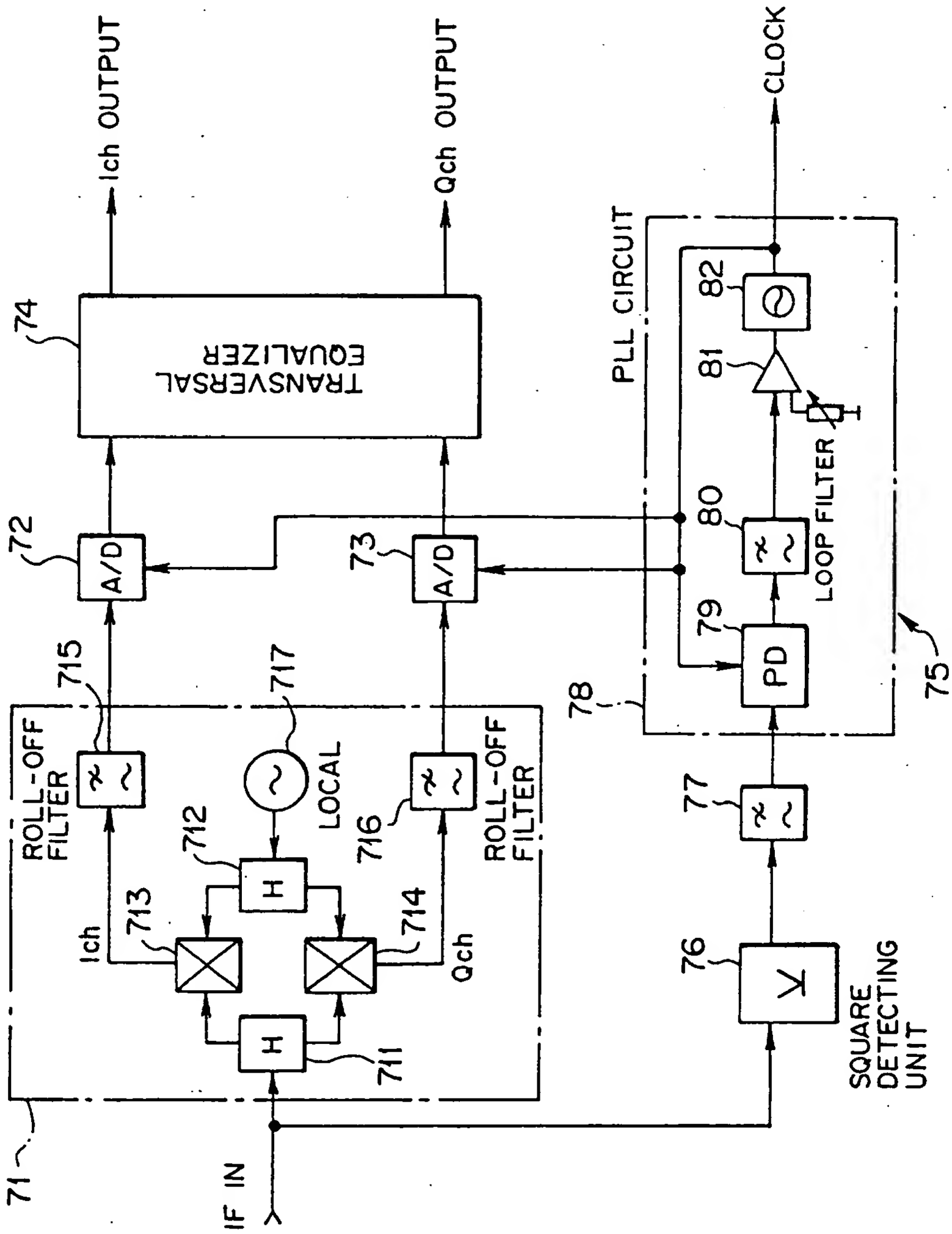

ADJUSTMENT/NORMAL
Ich OUTPUT
Qch OUTPUT
271
272
27'
R
C
I
RANDOM PULSE
46'
SEL
642
64
474
473
47'
475
61
62
65
63
66
66'
65'
472
ERROR SIGNAL
PN PATTERN GENERATING UNIT
471
671
COUNTER
HIGH-SPEED CLK CLK
CLEAR
A/D
23
24
227
THE POSITION WHERE THE TRANSVERSAL EQUALIZER IS ARRANGED.
28'
296
67:CONVERTING CIRCUIT
22
ROLL-OFF FILTER
Ich
Qch
225
226
222
LOCAL
223
221
224
IF IN

FIG.60
PRIOR ART



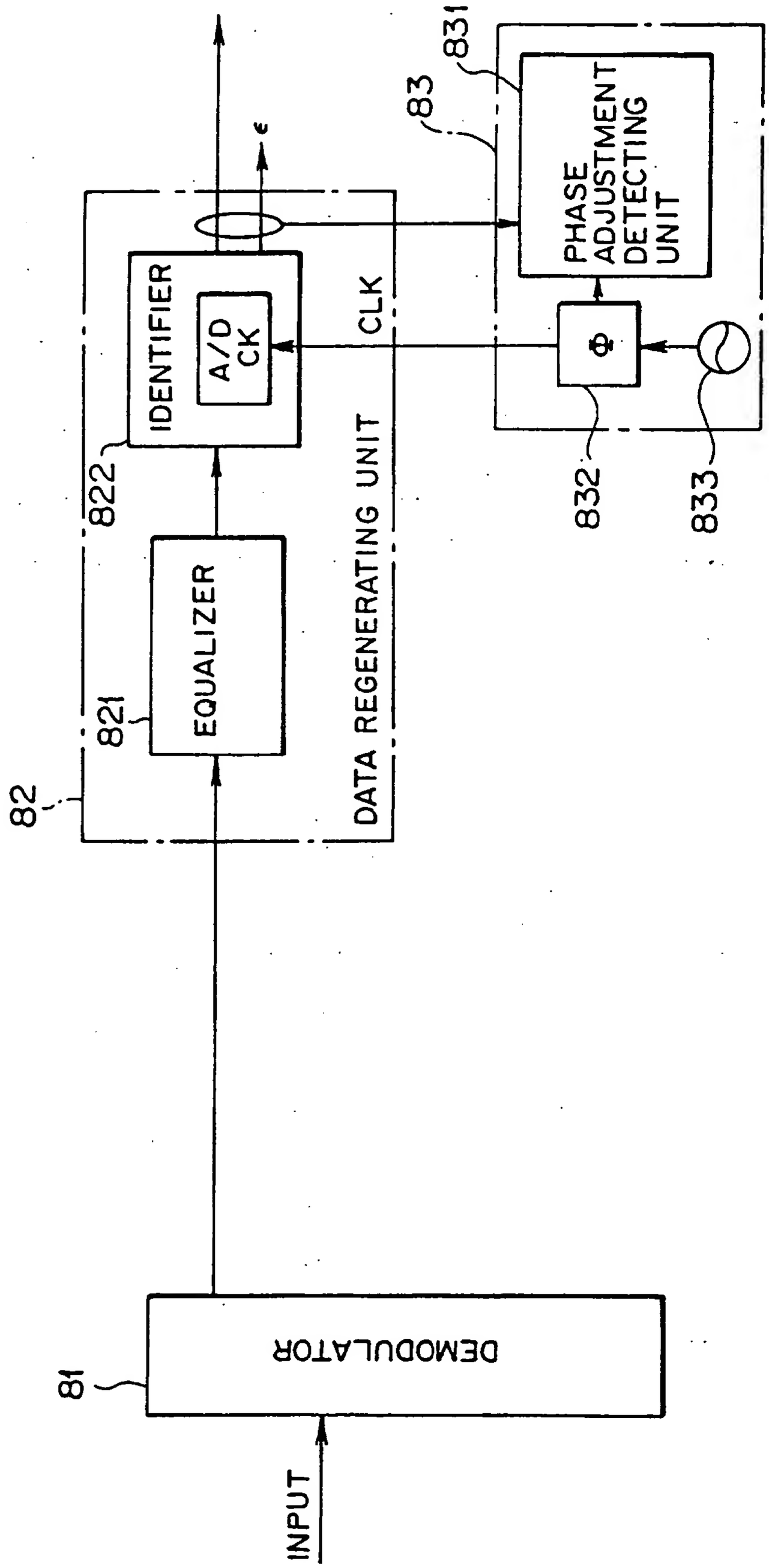


FIG. 61
PRIOR ART